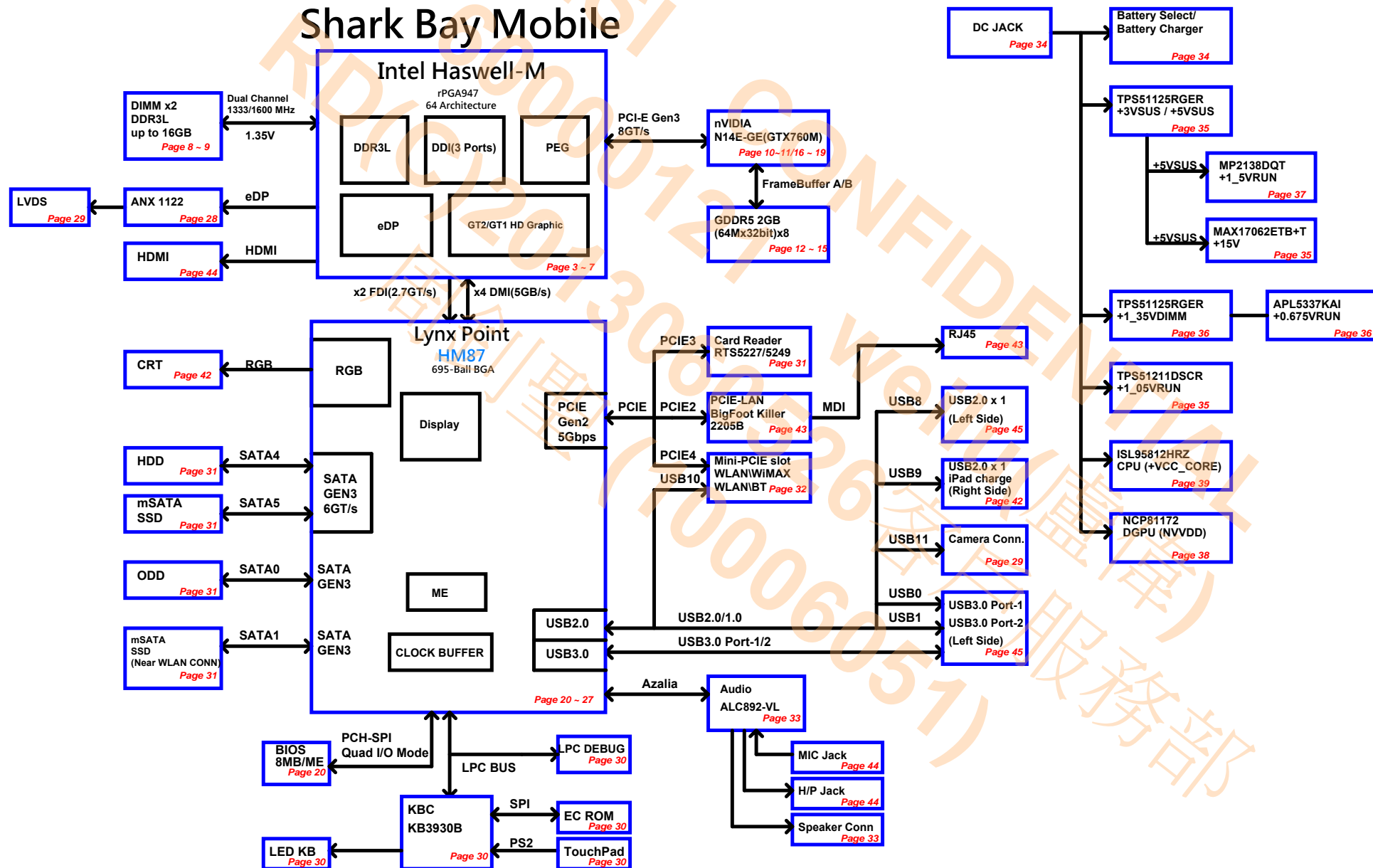


MS-16GC ver:0A

Shark Bay Mobile



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

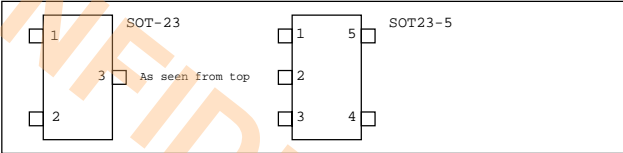
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.2V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVDD	0.6~1.2V(VBoot:0.9V)Core Voltage for nVIDIA N14E-GE DGPU	GPIO11_GPUVID
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

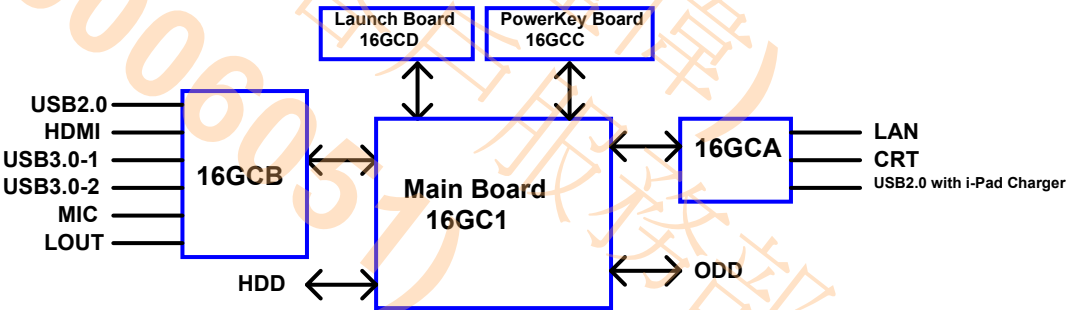
PCB Footprints



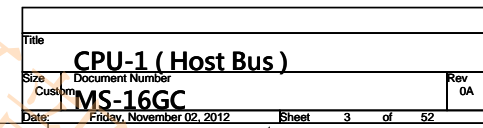
POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high



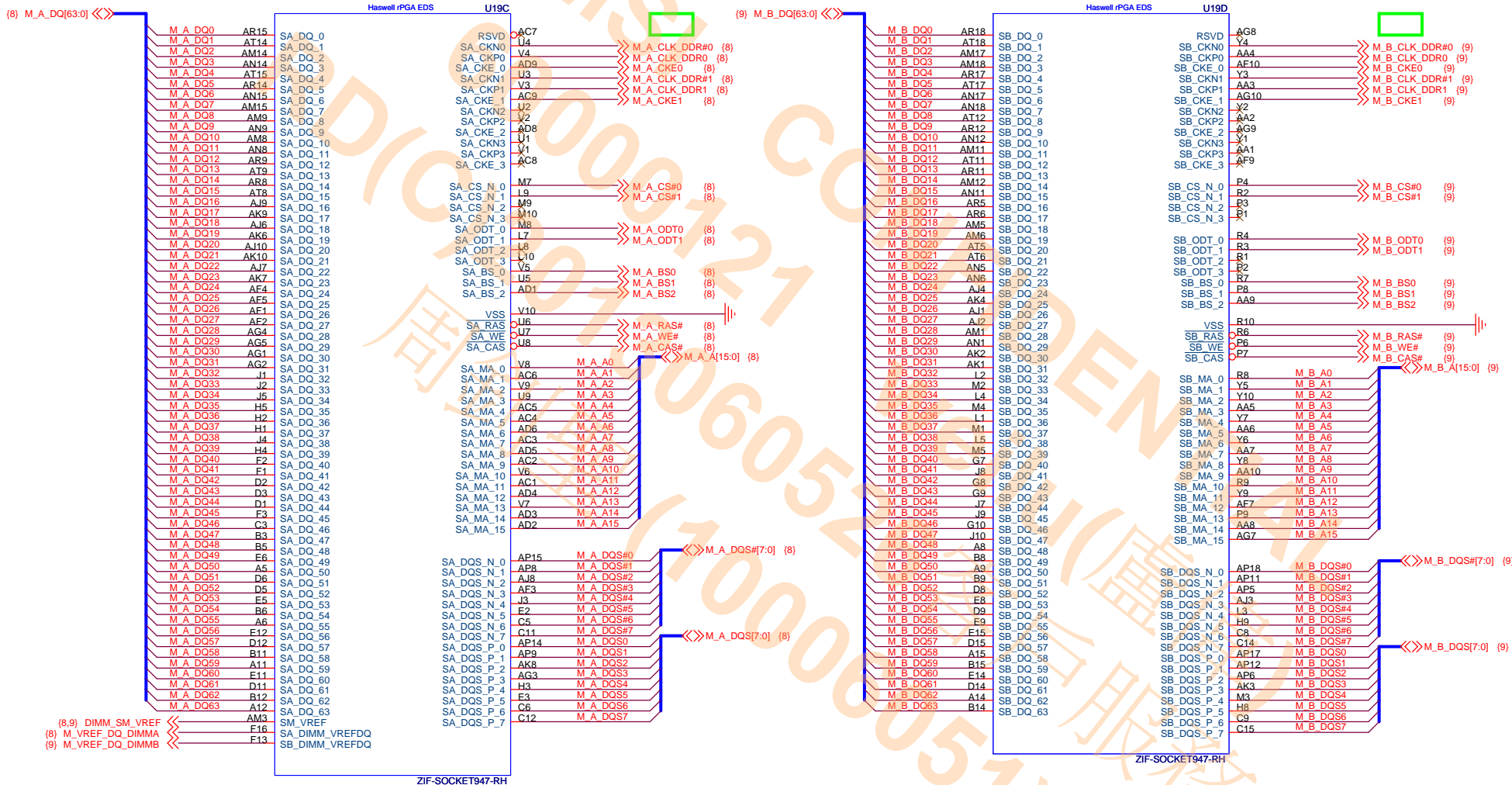
Haswell (CLK,MISC,JTAG)



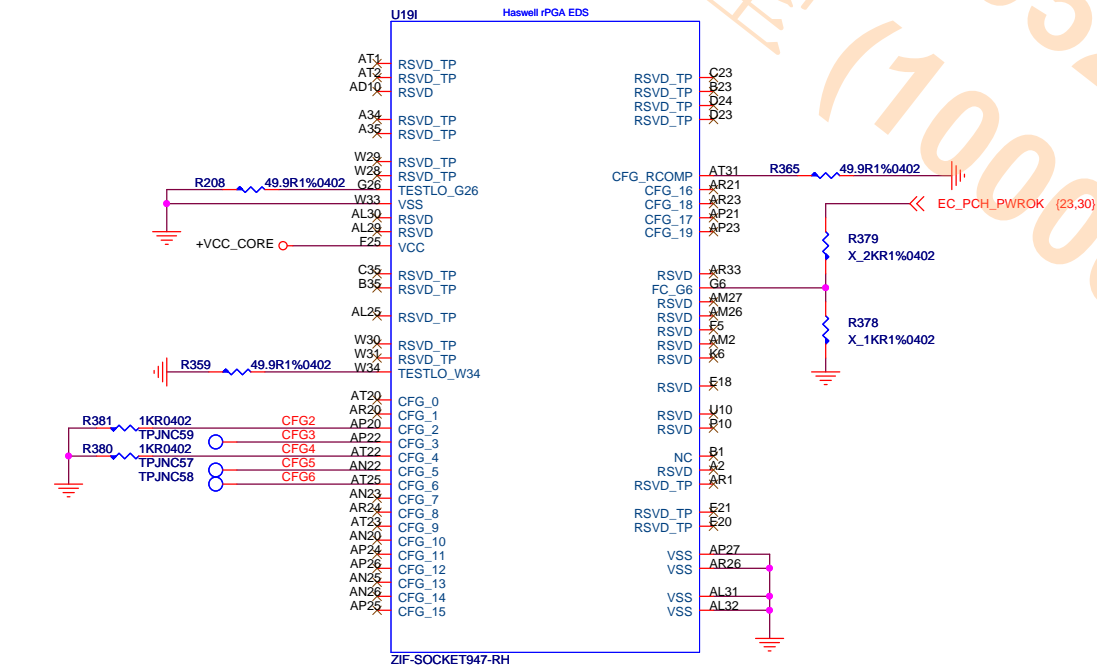
Haswell (DDR3L)

SODIMM#A

SODIMM#B

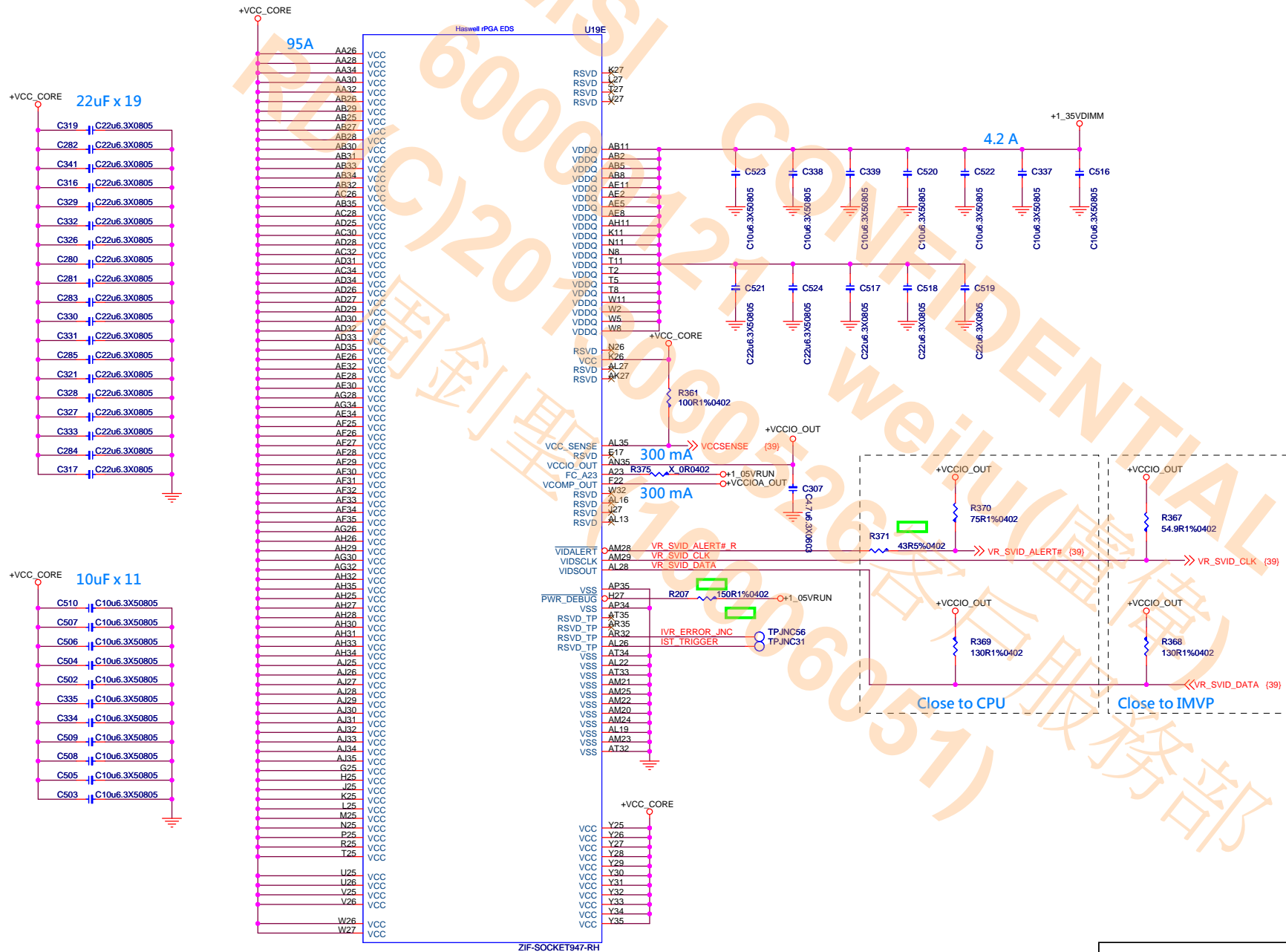


Haswell (Reserved)



PCI Express* Static x16 Lane Number Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden
eDP enable	
CFG4	1 = Disabled 0 = Enabled
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express
PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Haswell (POWER)

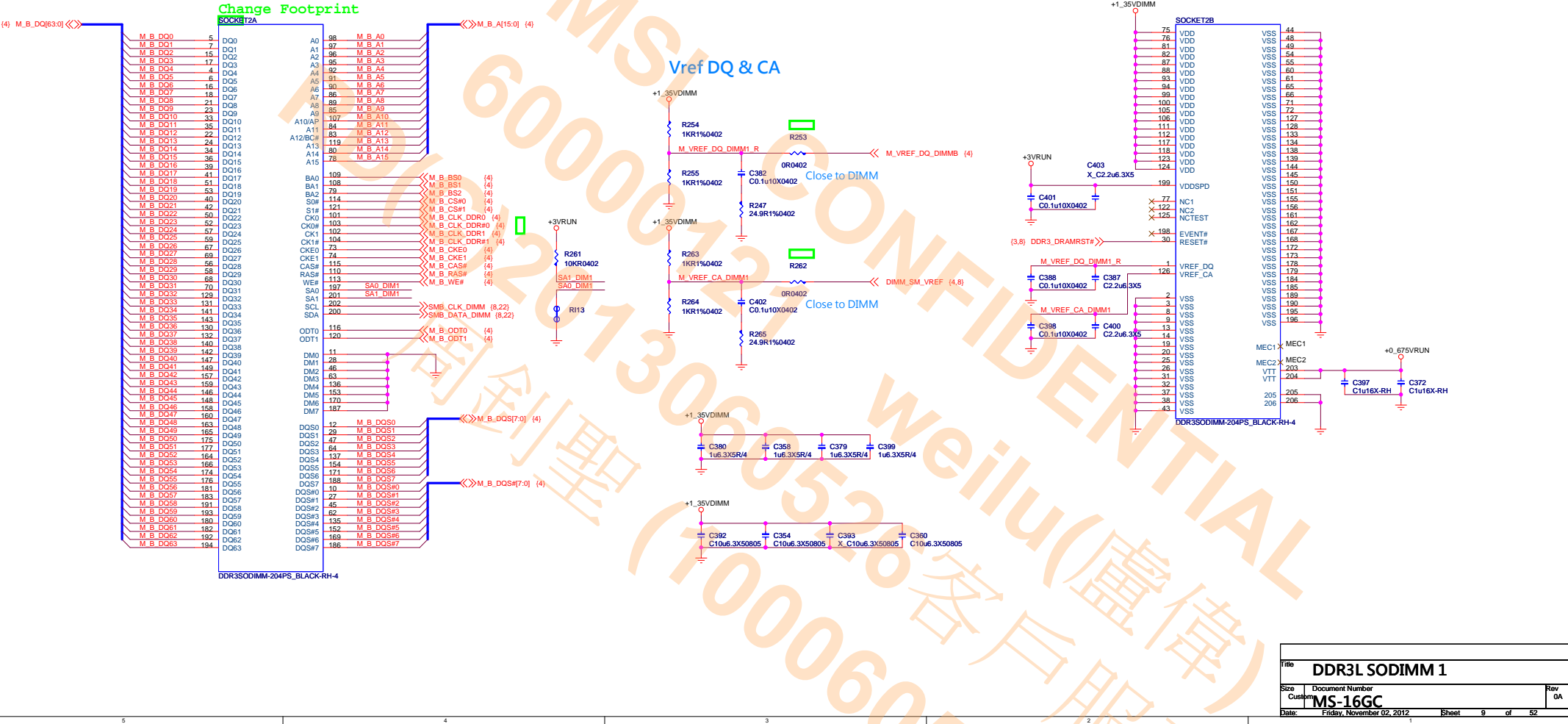


Haswell (GND)

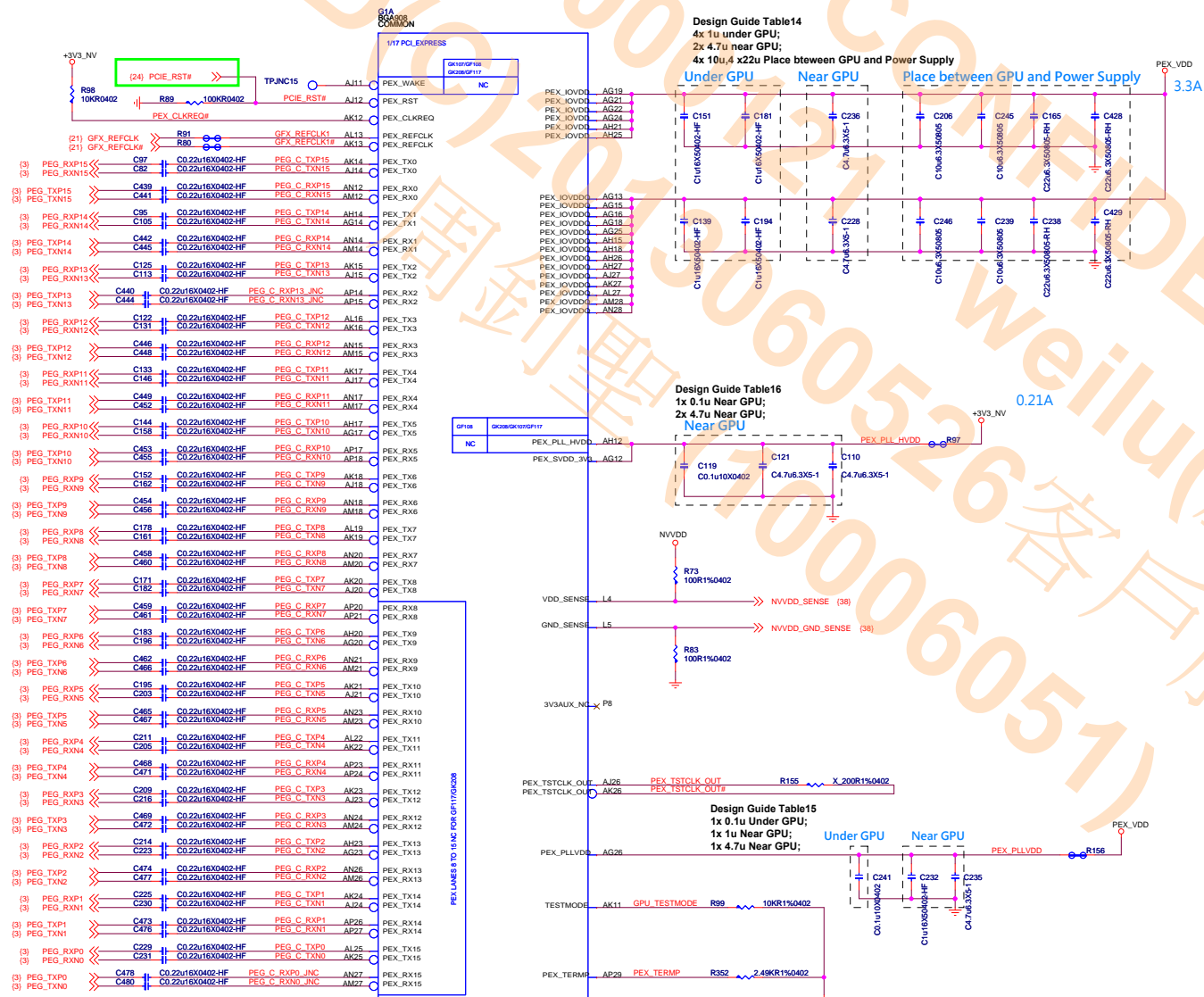
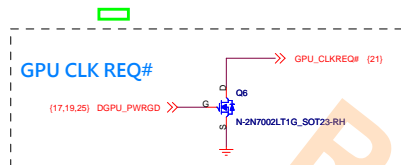


Title			
DDR3L SODIMM 0			
Size	Document Number		Rev
Custom	MS-16GC		0A
Date:	Friday, November 02, 2012	Sheet	8 of 52

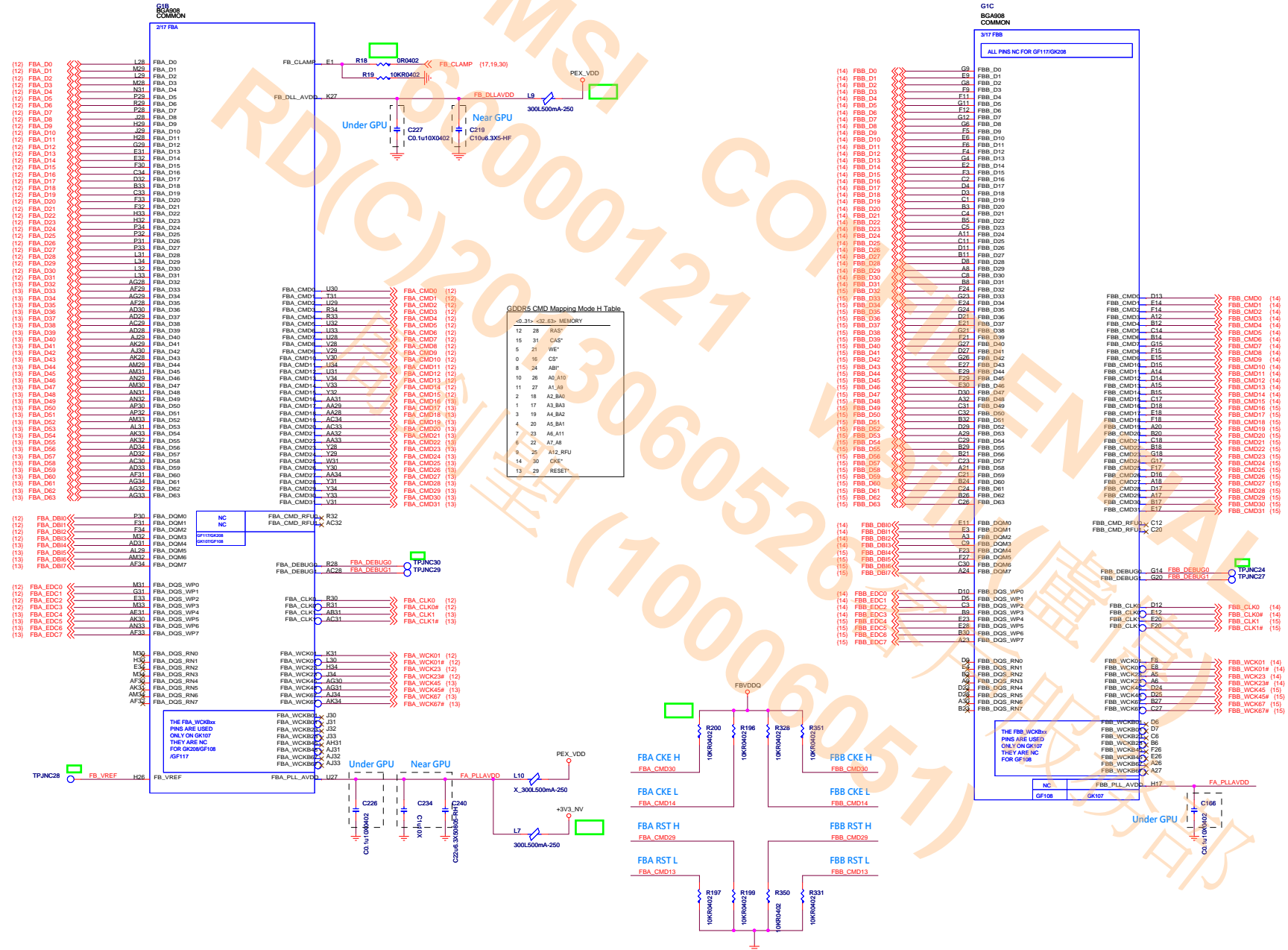
SODIMM#B



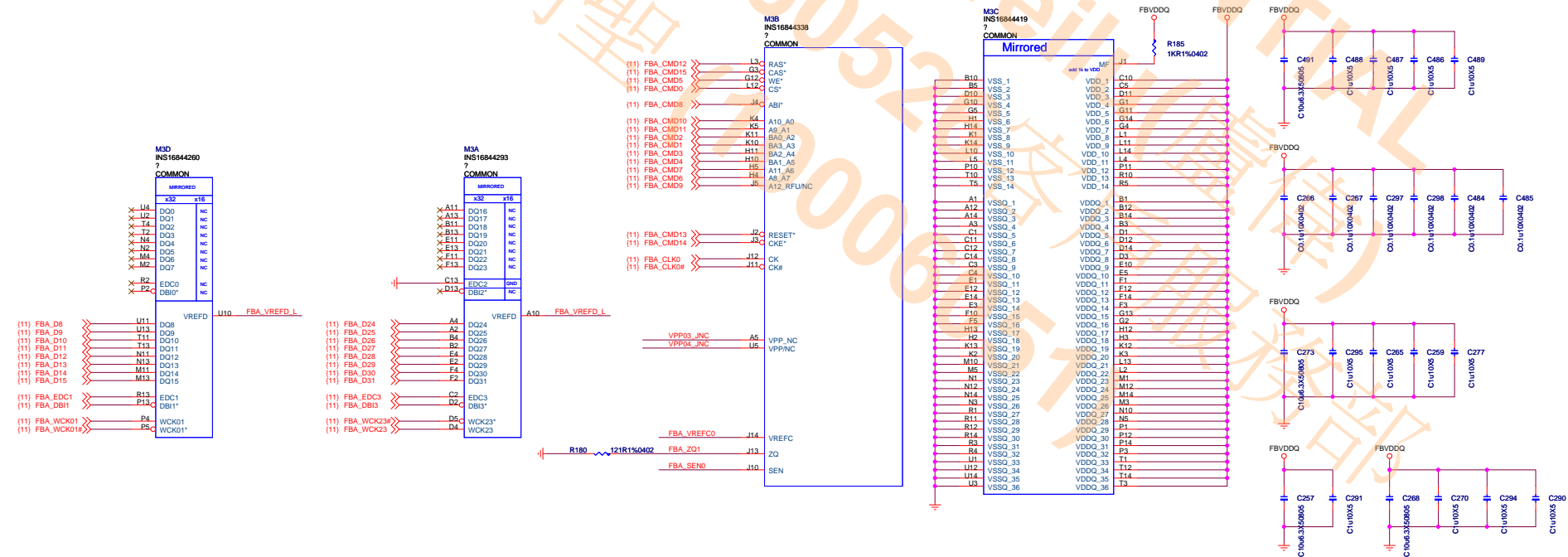
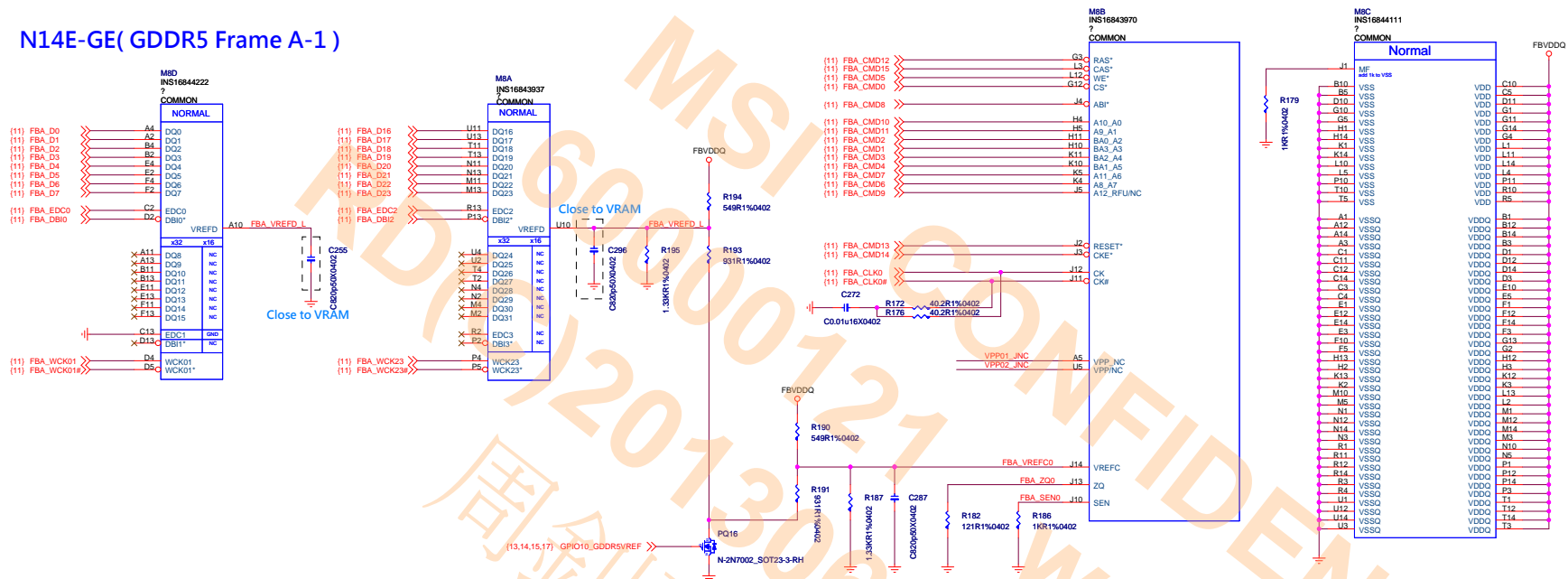
N14E-GE(PCI-Express Gen3 x16 Interface)



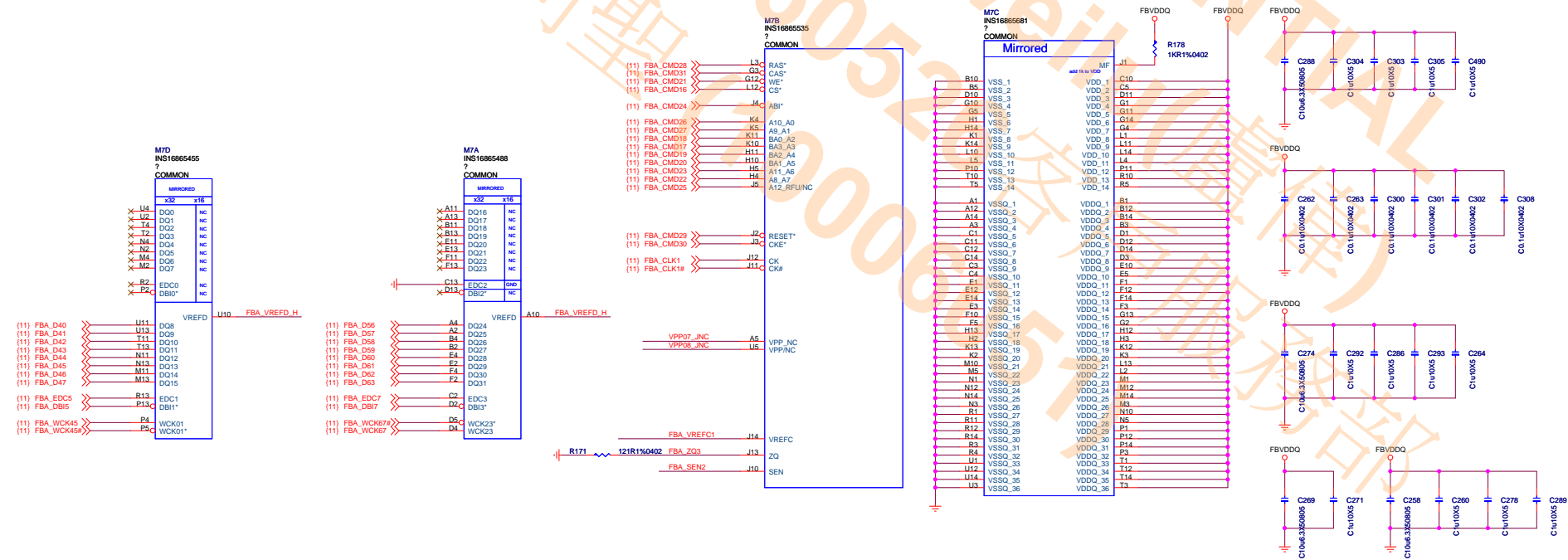
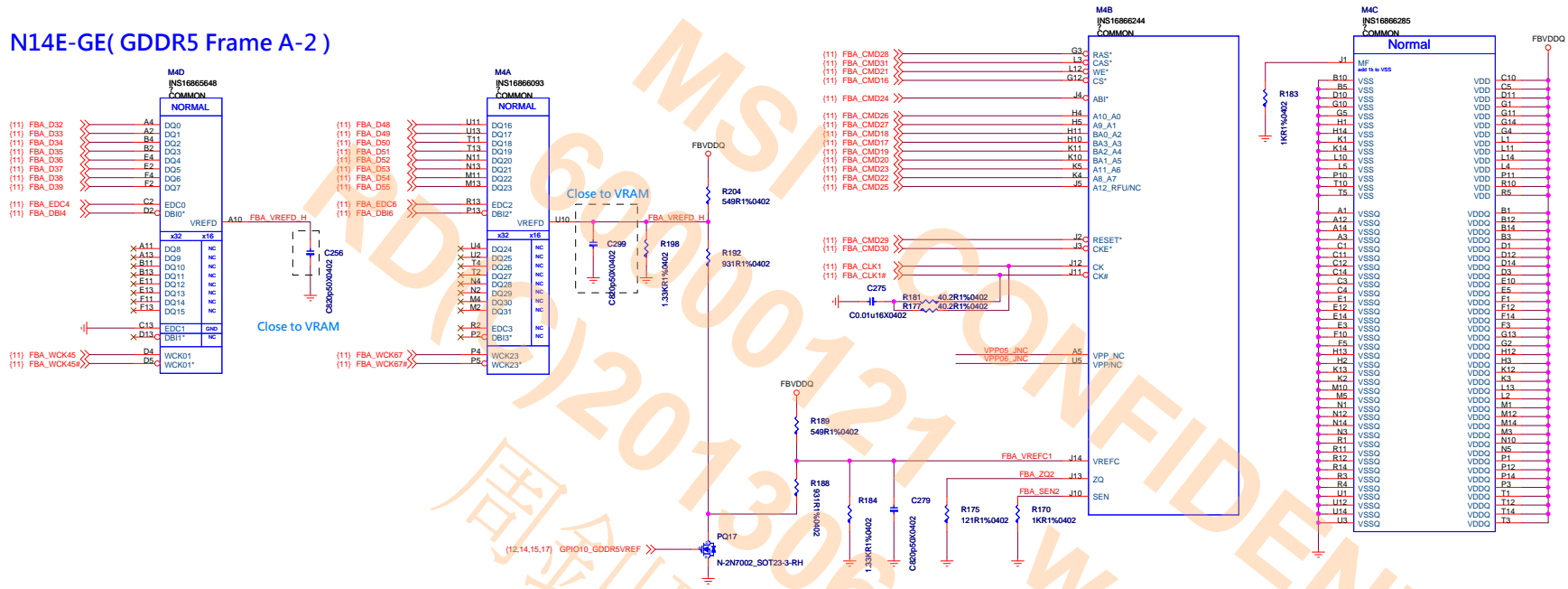
N14E-GE(Frame Buffer Interface)



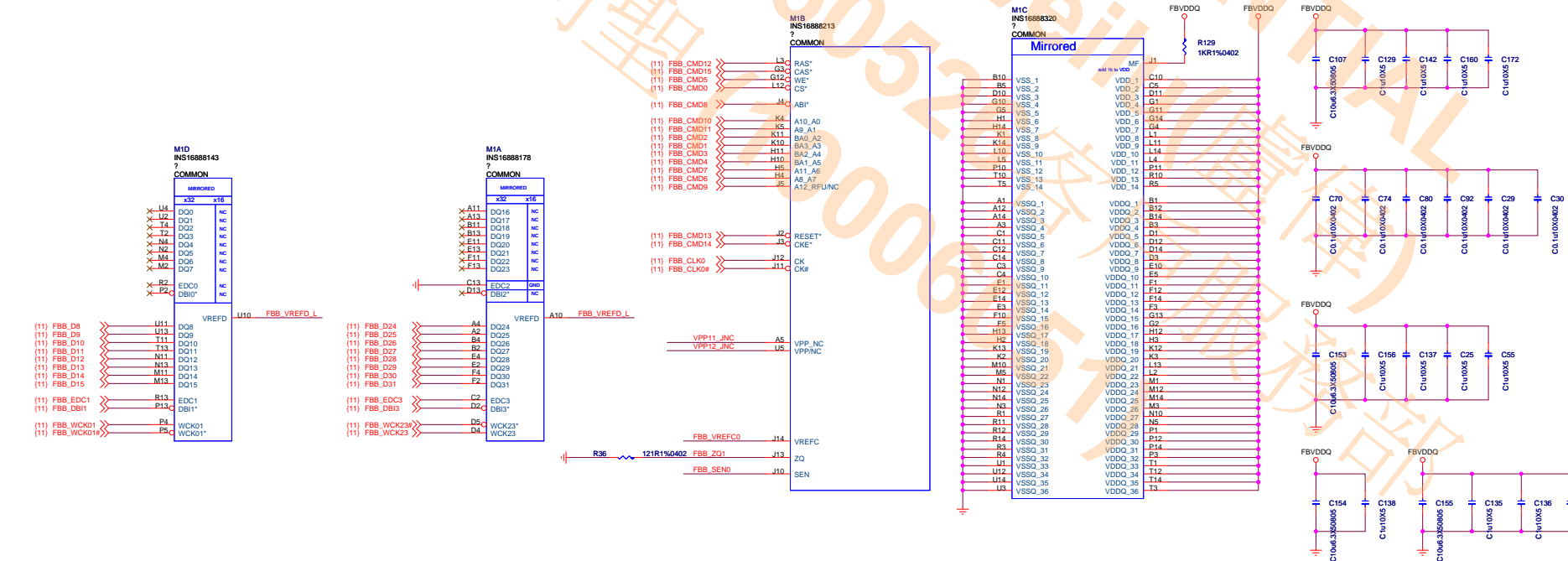
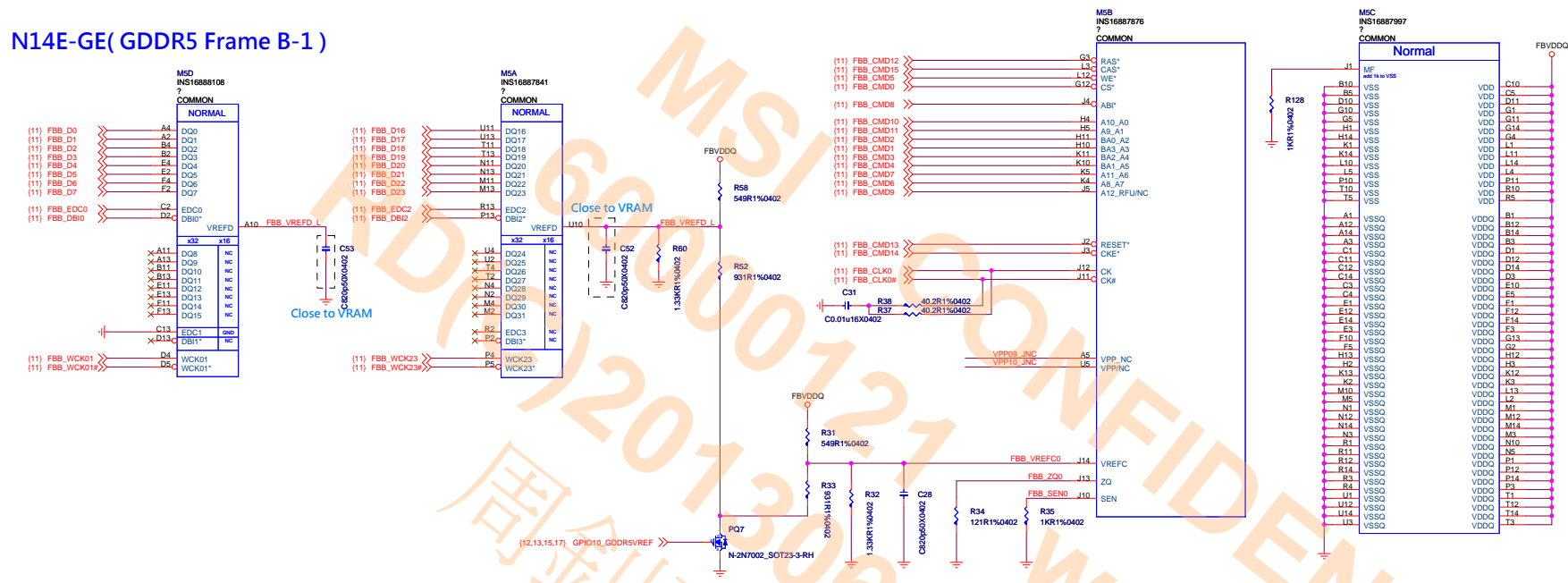
N14E-GE(GDDR5 Frame A-1)



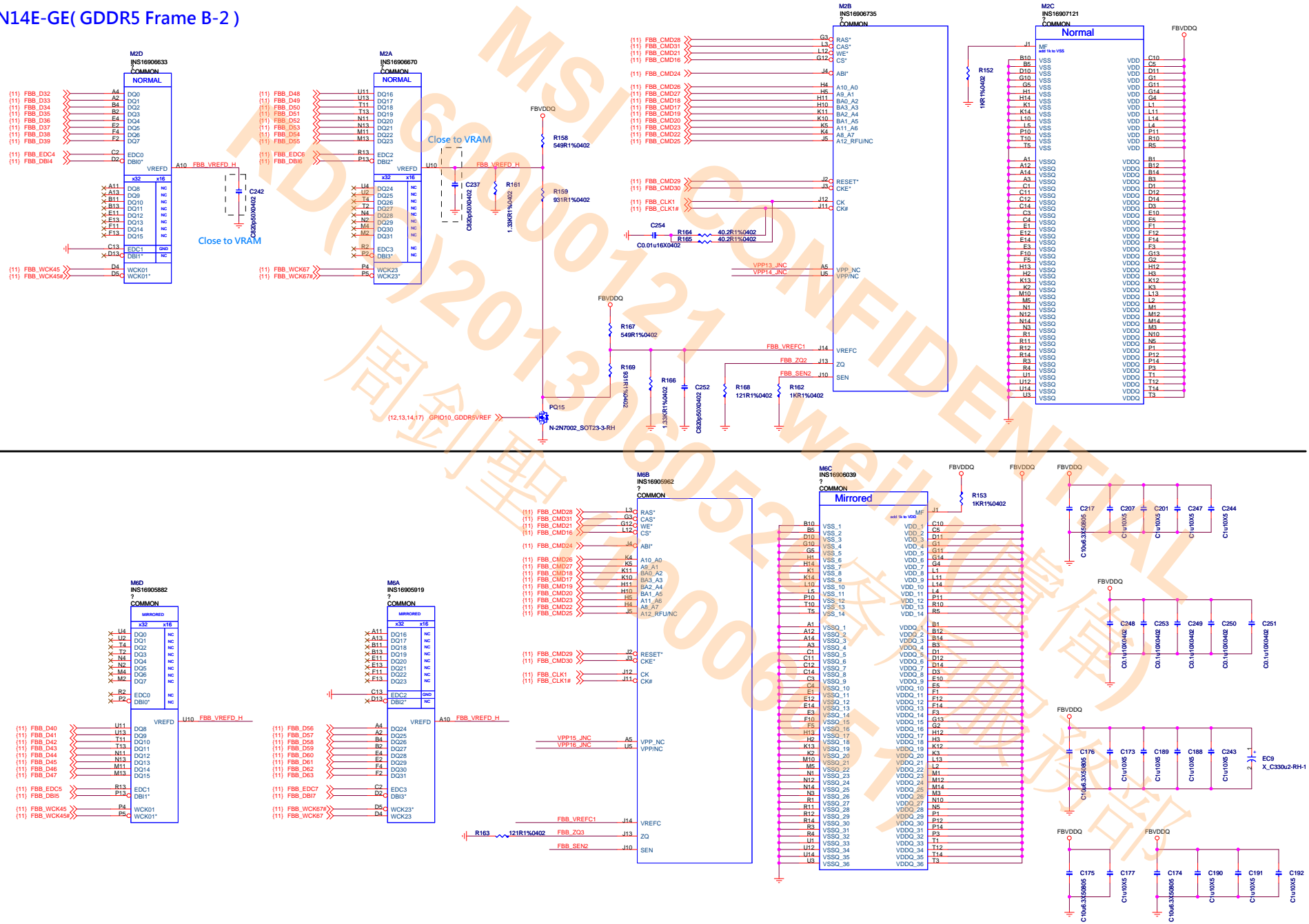
N14E-GE(GDDR5 Frame A-2)



N14E-GE(GDDR5 Frame B-1)

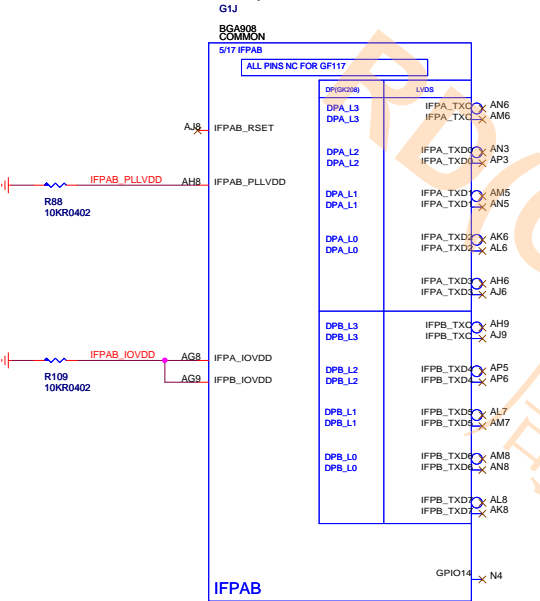


N14E-GE(GDDR5 Frame B-2)

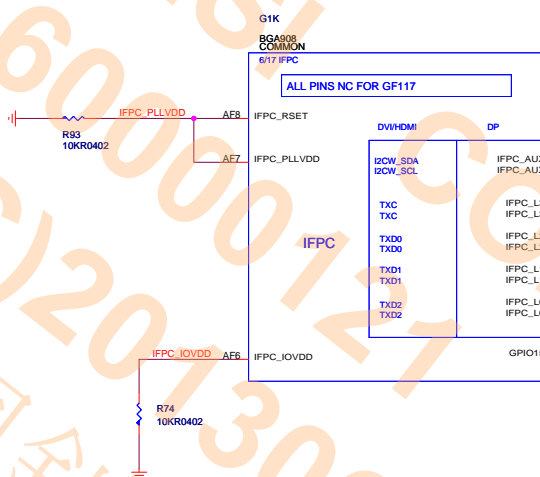


N14E-GE(Display IF)

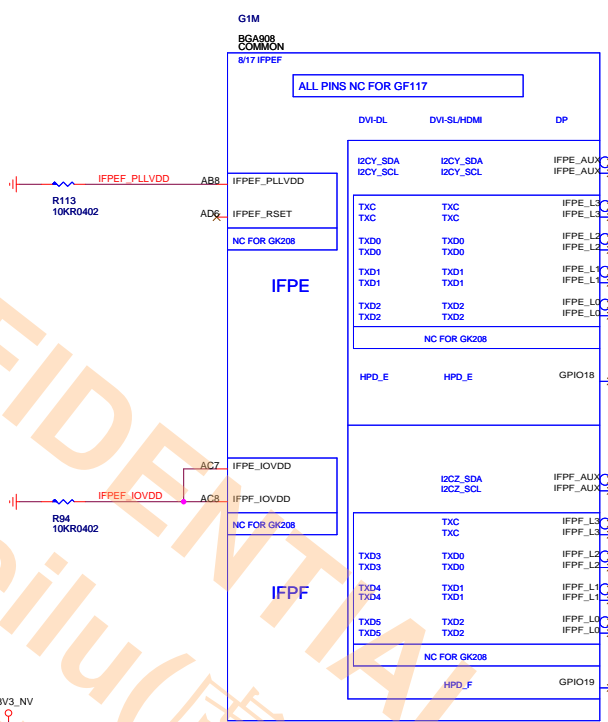
IFP A/B LVDS Dual Link



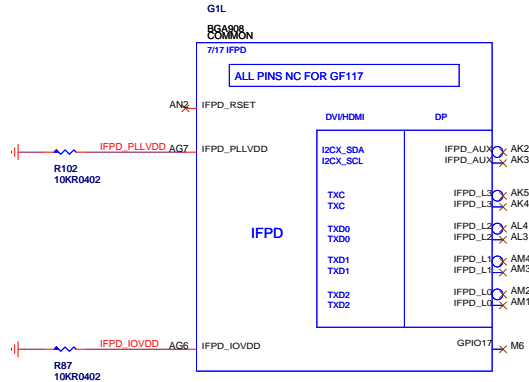
IFP C Native HDMI OR DP



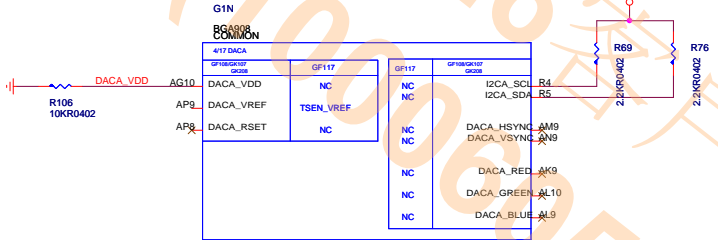
IFP E/F Dual Link TMDS DVI-I



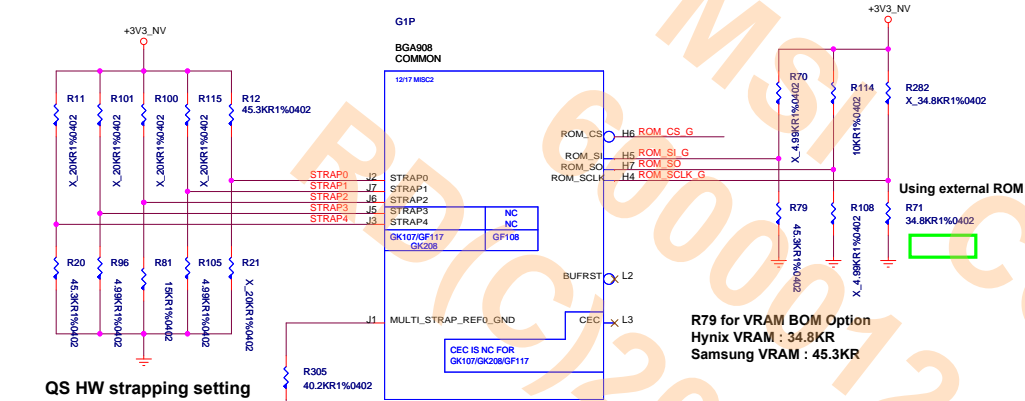
IFP D Dual Mode DP



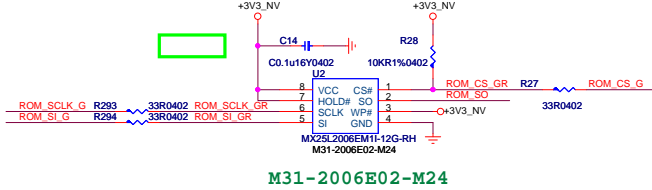
DAC A VGA



N14E-GE(Thermal & GPIO)

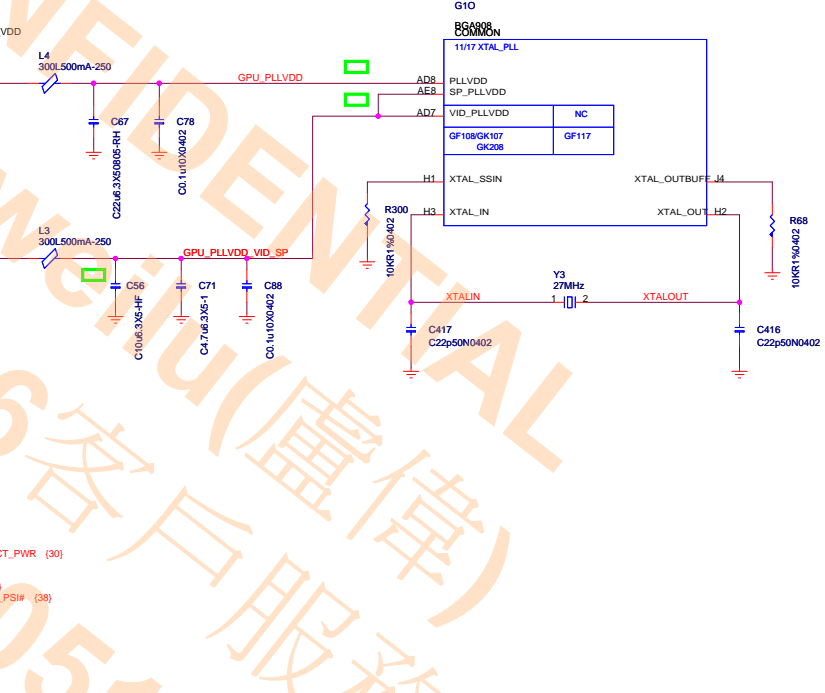
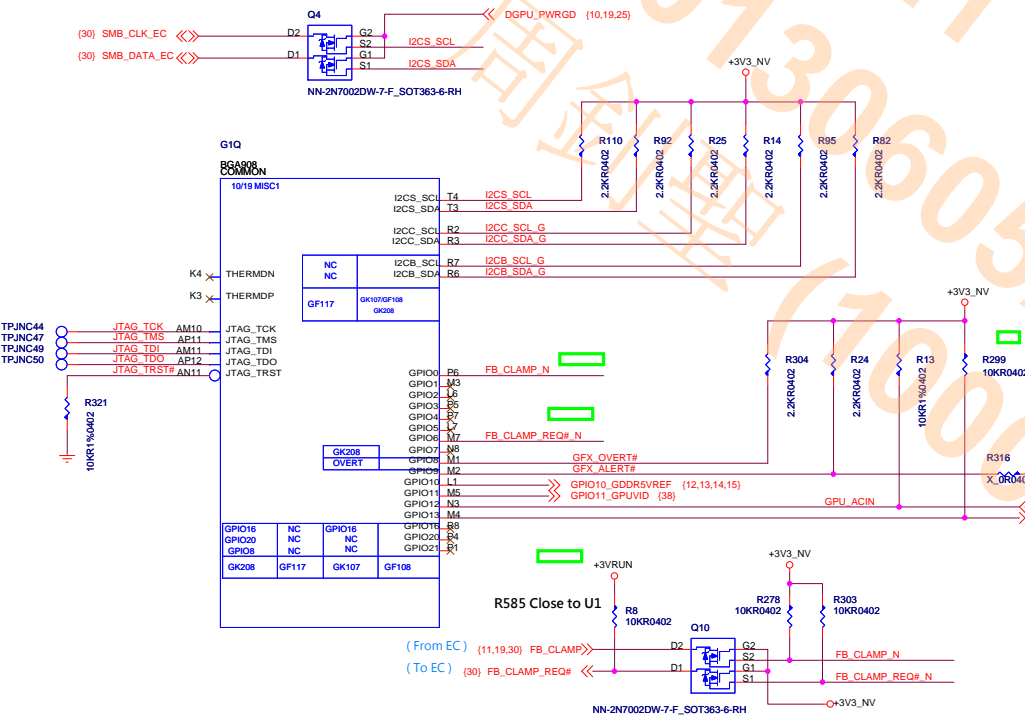


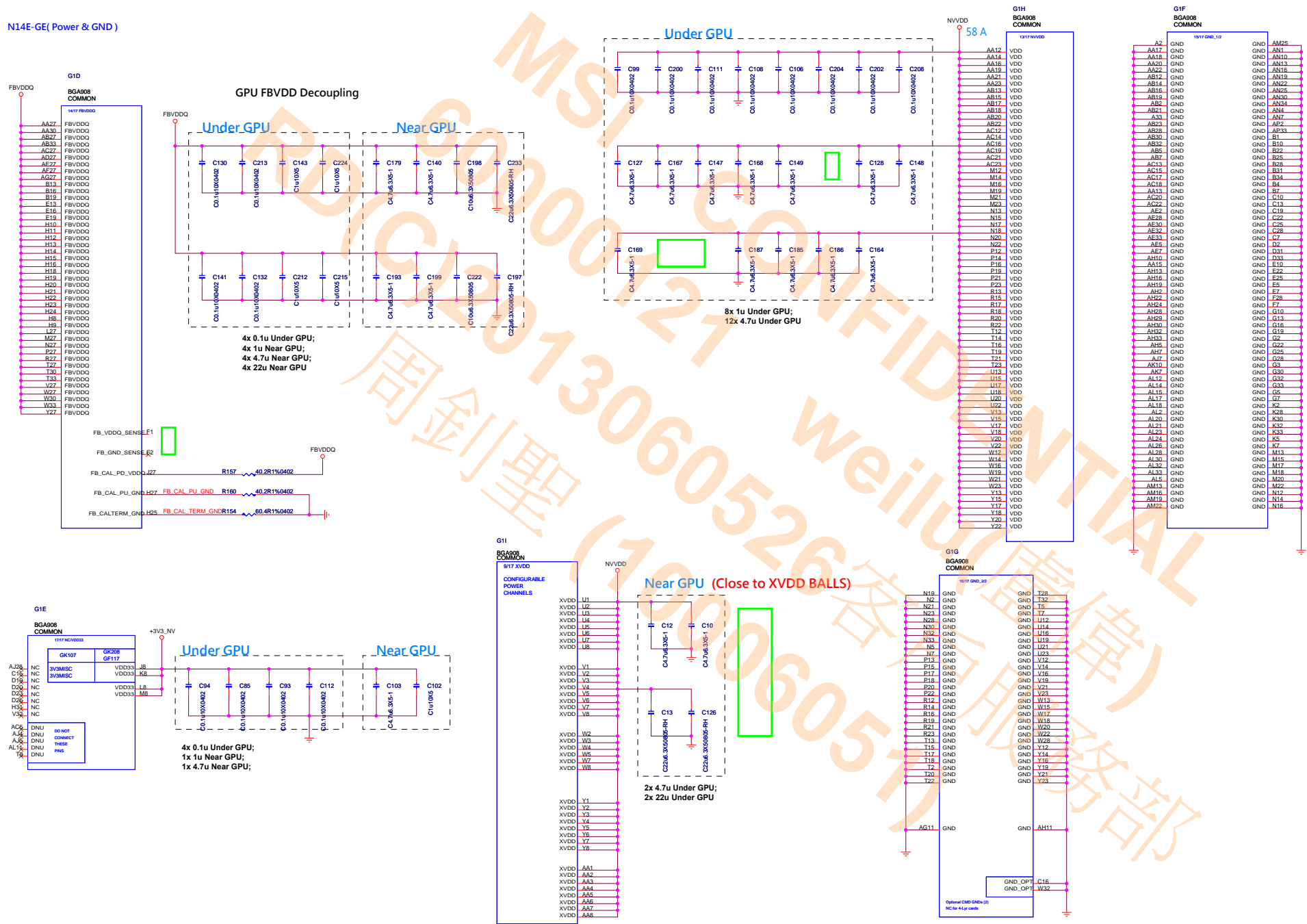
External EEPROM



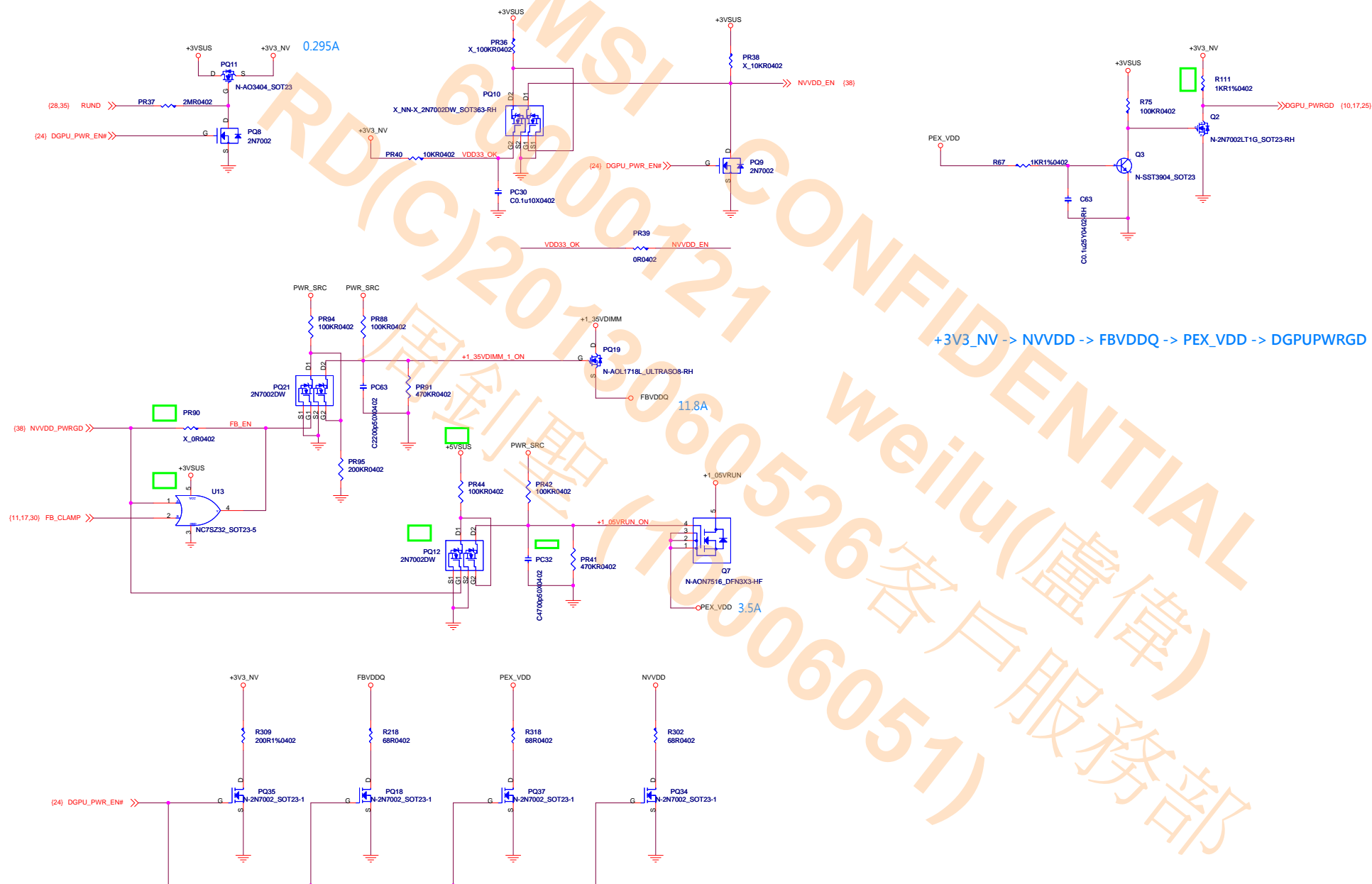
M31-2006E02-M24

QS HW strapping setting



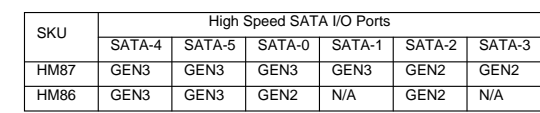


N14E-GE(Power Control)



Title		N14E-GE Power Control	
Size	Document Number	Rev	
Custom	MS-16GC	OA	
Date:	Friday, November 02, 2012	Sheet	19 of 52

RTC_BAT
BAT2
D06-0100300-K26



SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

ODD — SATA GEN2

m-SATA — SATA GEN3
(Near WLAN CONN)

```

graph LR
    HDD[HDD] --- SATA_GEN3[SATA GEN3]
    mSATA[m-SATA SSD] --- SATA_GEN3

```

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

Reserved for Codec use RUN

ed for Codec use RUN +3VSUS

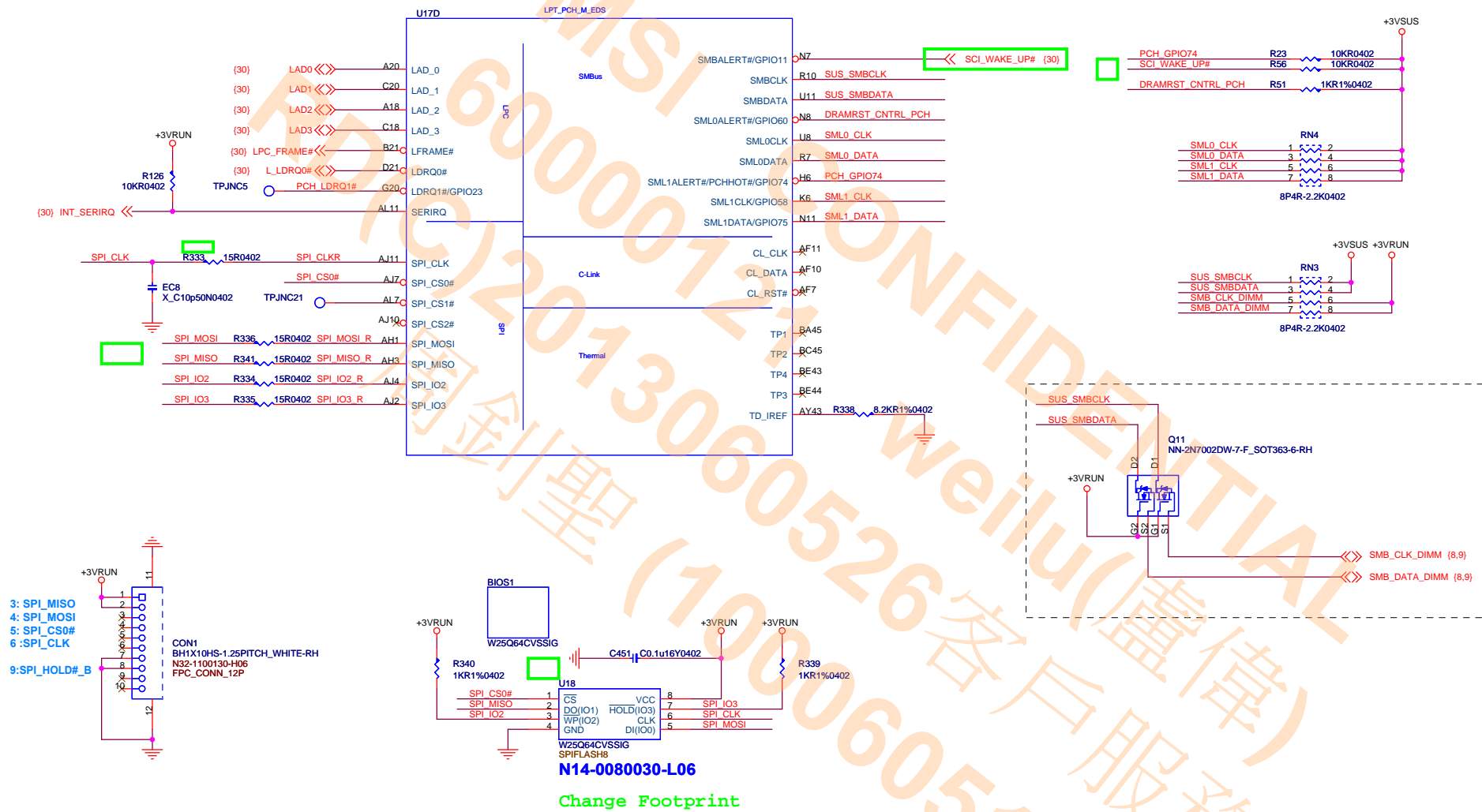
R284
X_1KR0402

HDA_SYNC_PCH_R

Ref Schematic Design Checklist p.31

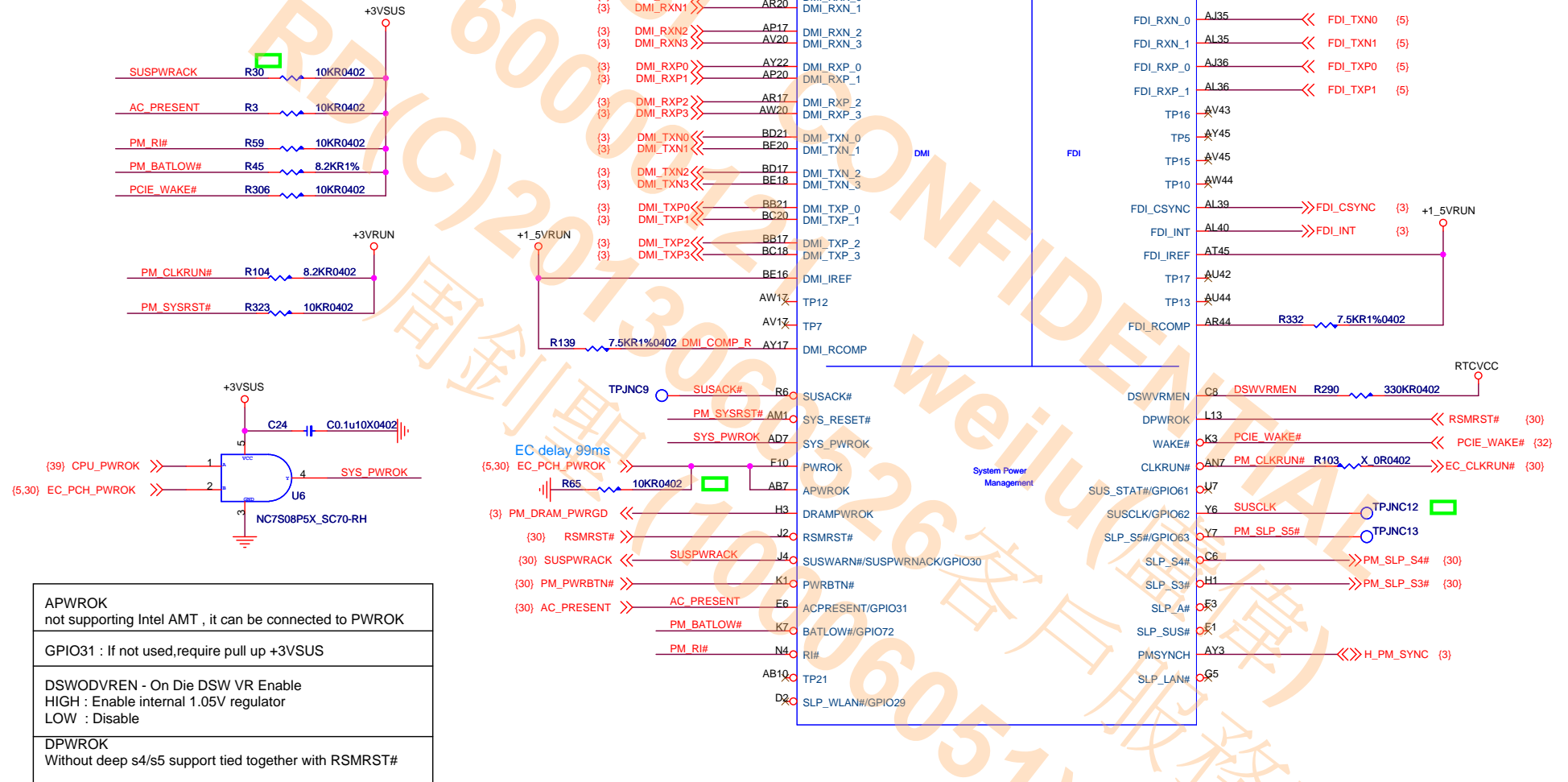
Lynx Point (Clock)

Lynx Point (LPC,SMBUS)



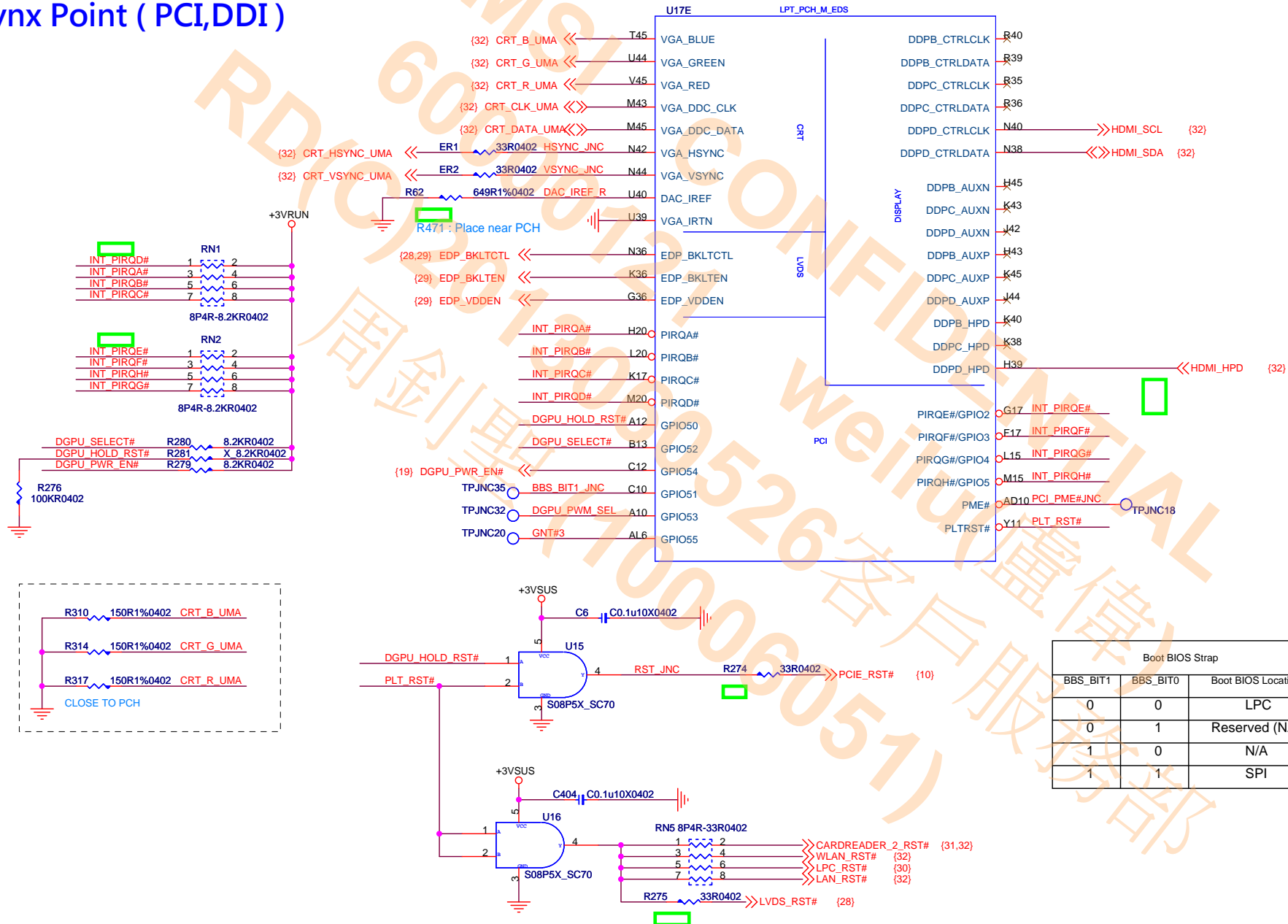
Title			
PCH-3 (LPC,SMBUS)			
Size	Document Number	Rev	
Custom	MS-16GC	0A	
Date:	Friday, November 02, 2012	Sheet	22 of 52

Lynx Point (DMI,FDI)



Title		PCH-4 (DMI,FDI)	
Size	Custom	Document Number	MS-16GC
Date:	Friday, November 02, 2012	Sheet	23 of 52
		Rev 0A	

Lynx Point (PCI,DDI)

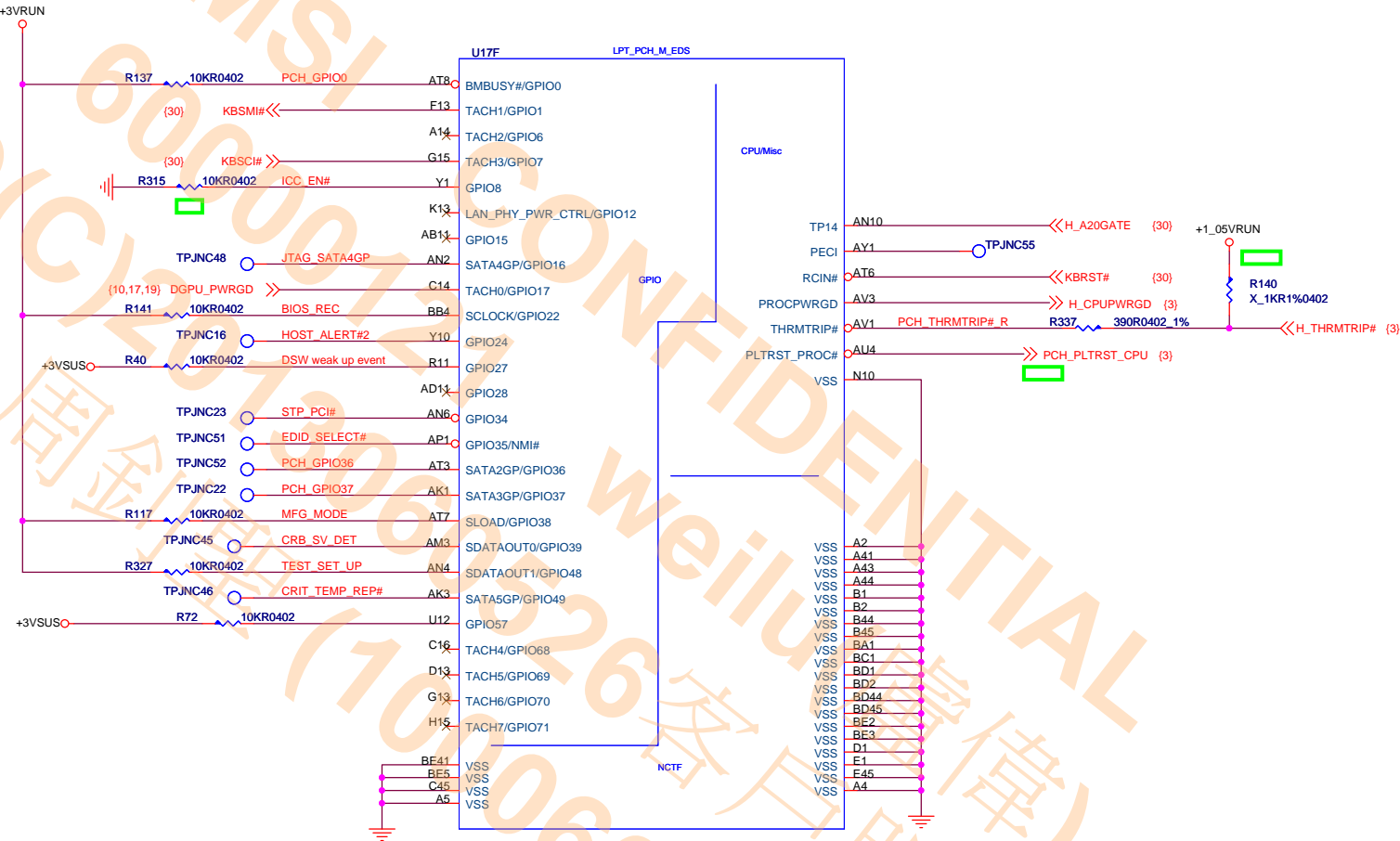


Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

Lynx Point (GPIO,MISC)

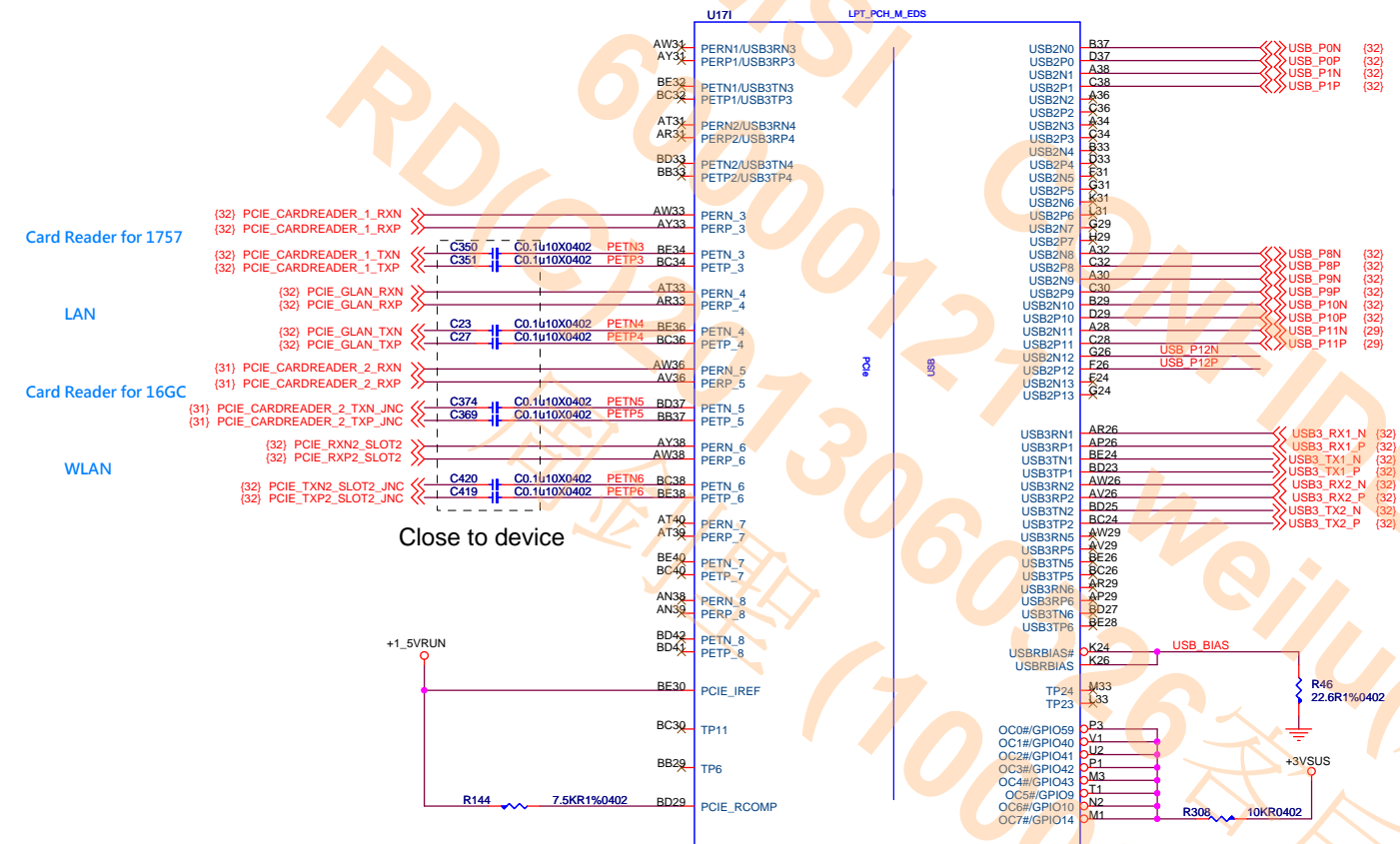
GPIO Setting : Ref 486708_LPT_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

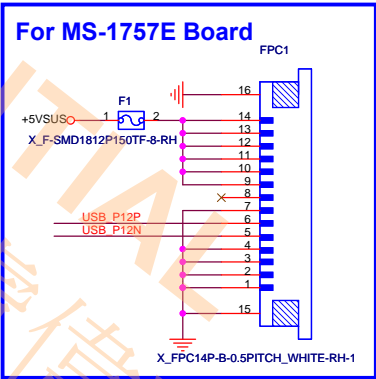


Title		PCH-6 (GPIO,MISC)	
Size	Document Number	MS-16GC	
Custom			
Date:	Friday, November 02, 2012	Sheet	25 of 52

Lynx Point (PCIE,USB)

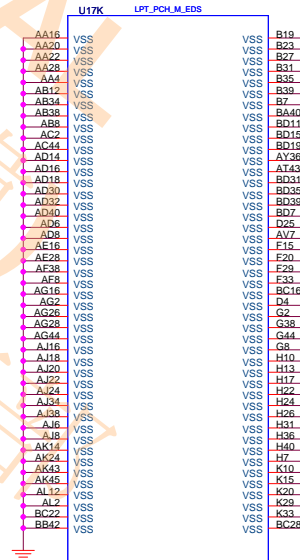


USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	(16GCB/1757B)
1	2	USB 3.0 Port 2	(16GCB/1757B)
2			NC
3			NC
4			NC
5			NC
6			NC
7			NC
8		USB 2.0 Port	(16GCB)
9		USB 2.0 Port	(16GCA/1757A)
10		WLAN	
11		WebCam	
12		USB 2.0 Port	(1757E)
13			NC
	3		NC
	4		NC
	5		NC
	6		NC

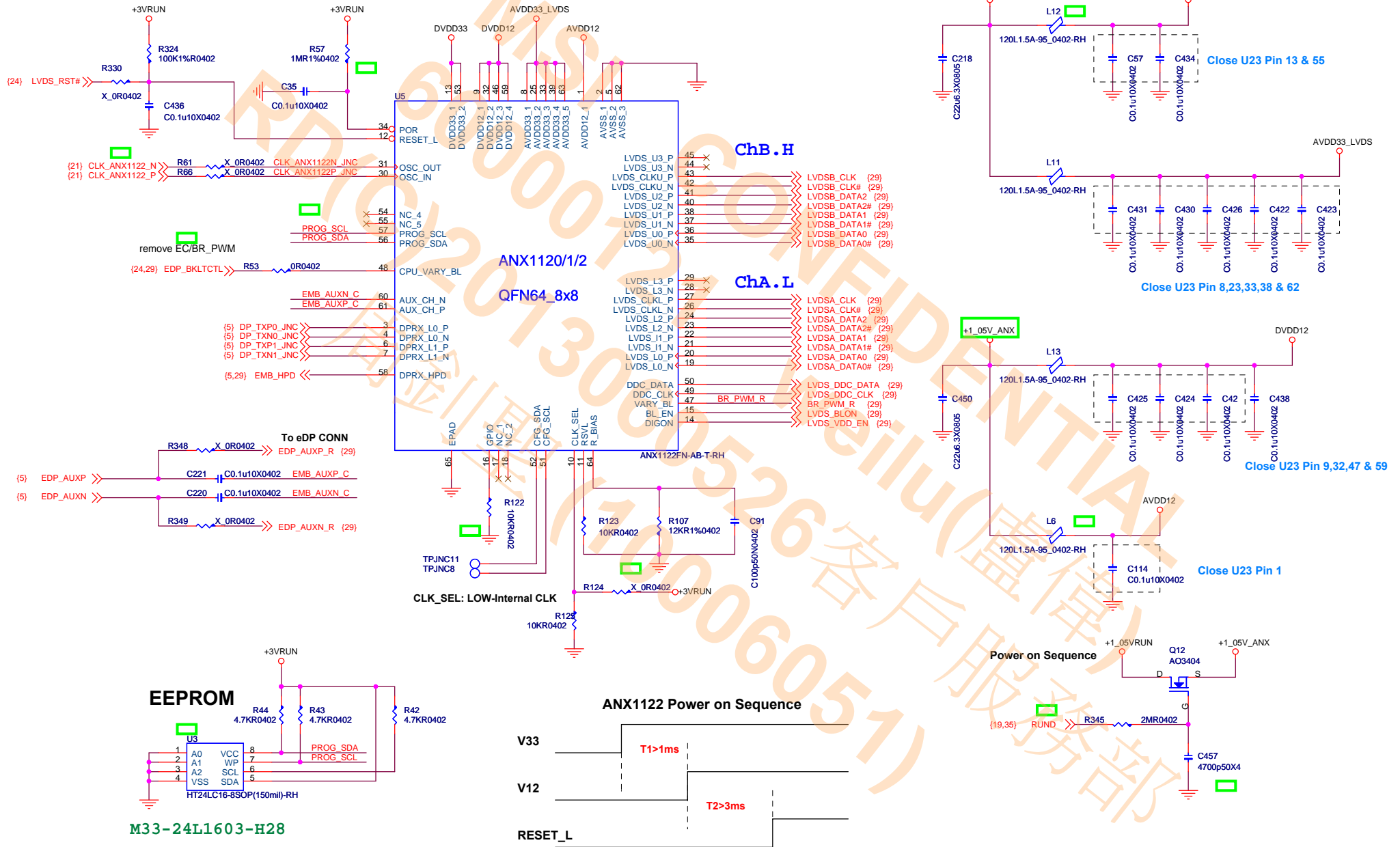


Title			
PCH-7 (PCIE,USB)			
Size	Document Number	Rev	
Custom	MS-16GC	0A	
Date:	Friday, November 02, 2012	Sheet	26 of 52

Lynx Point (Power)

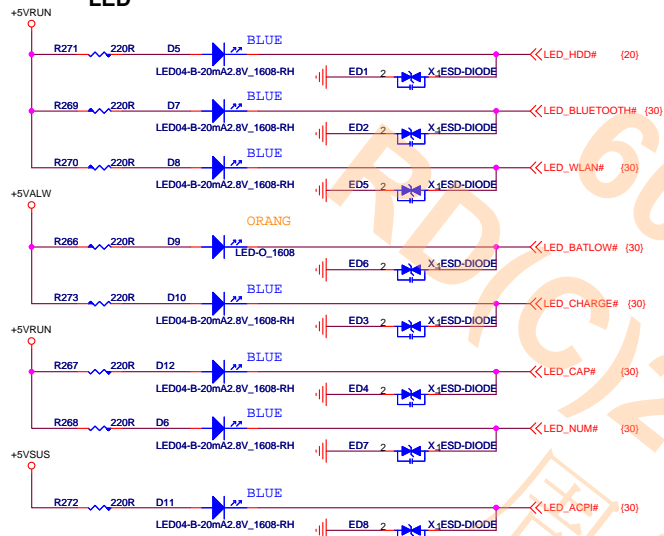


eDP to LVDS

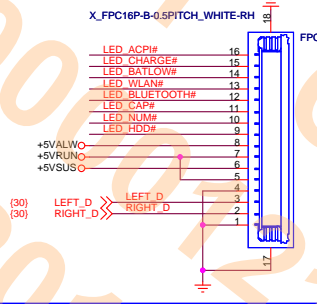


Title		
eDP to LVDS (ANX1122)		
Size	Document Number	Rev
Custom	MS-16GC	0A
Date:	Friday, November 02, 2012	Sheet 28 of 52

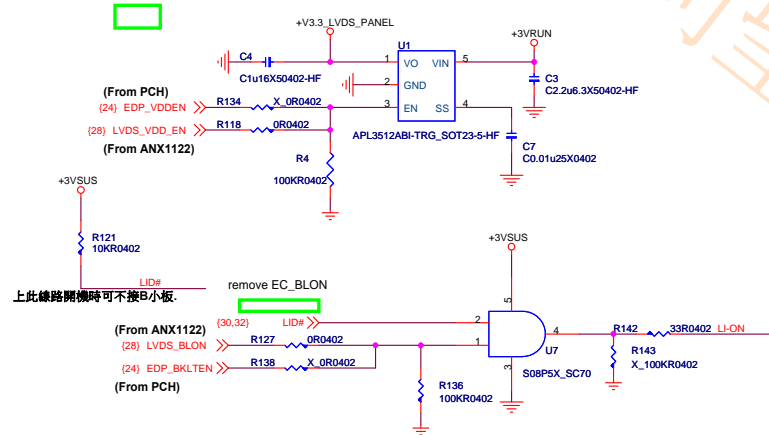
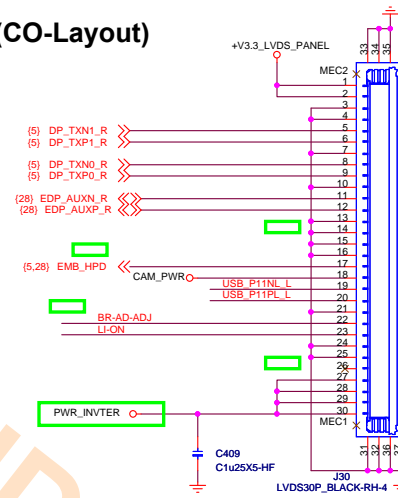
LED For 16GC1



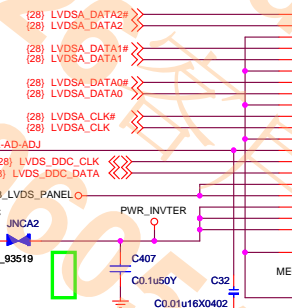
For MS-1757D board



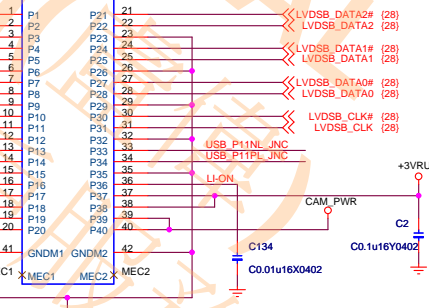
eDP CONN (CO-Layout)



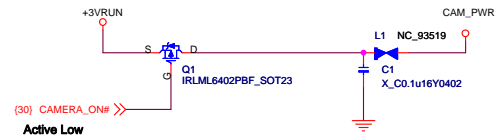
ChA.L



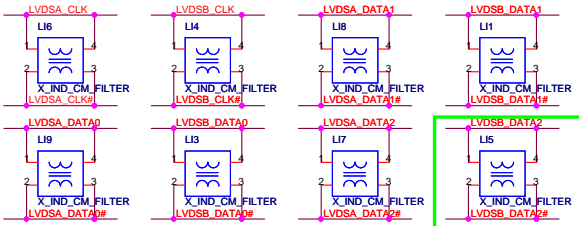
ChB.H



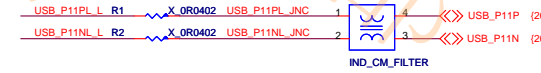
CAMERA

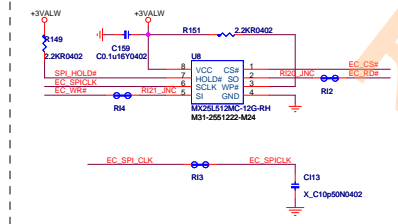


Reserved for EMI



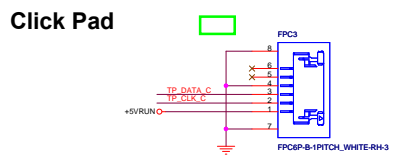
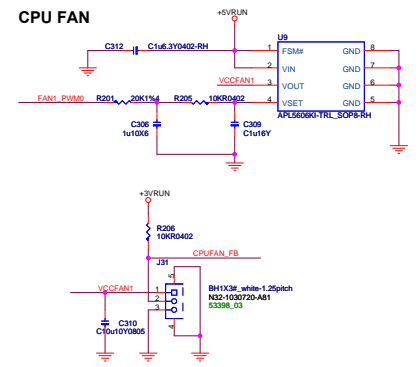
Reserved for EMI





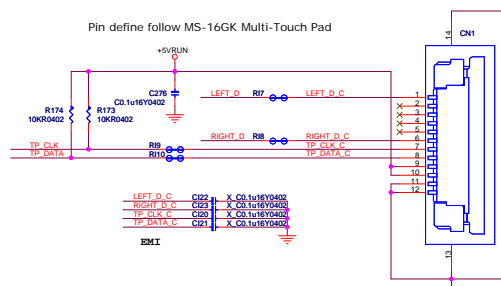
For SW Debug (LPC)

(22) L_LDR00#
(21) CLK_PCF_PORTB0

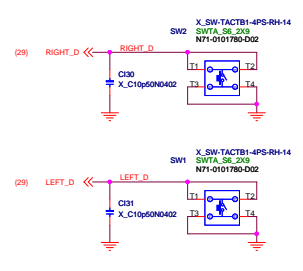


Touch Pad

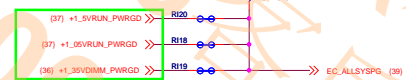
Pin define follow MS-16GK Multi-Touch Pad



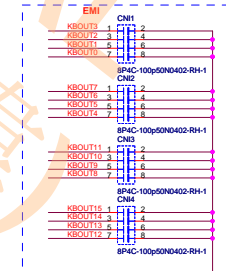
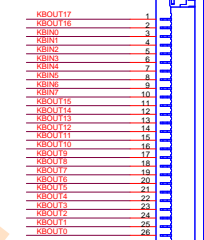
For 16GCI



remove TP Lock

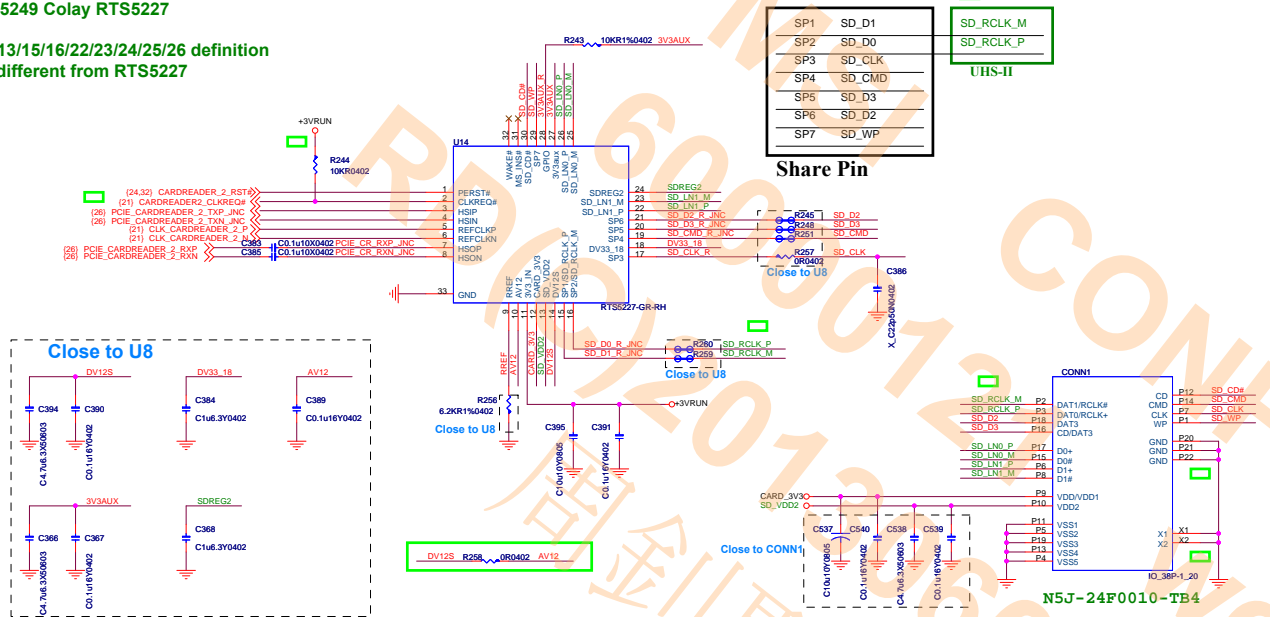


Keyboard conn

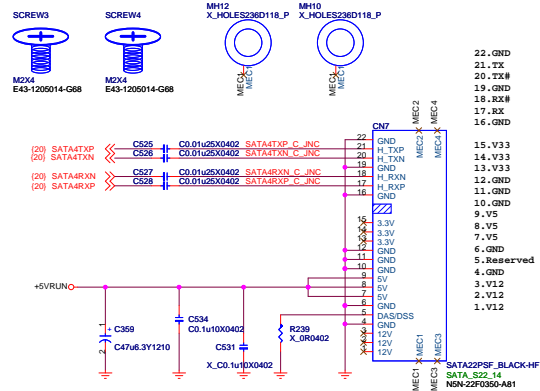


RTS5249 Colay RTS5227

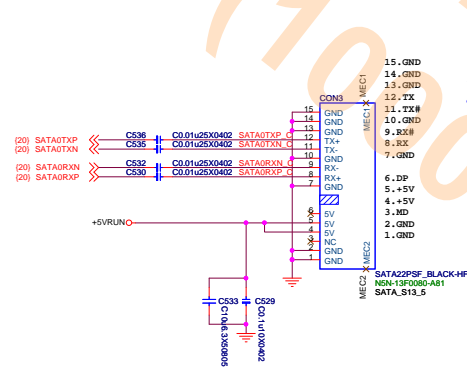
**Pin 13/15/16/22/23/24/25/26 definition
are different from RTS5227**



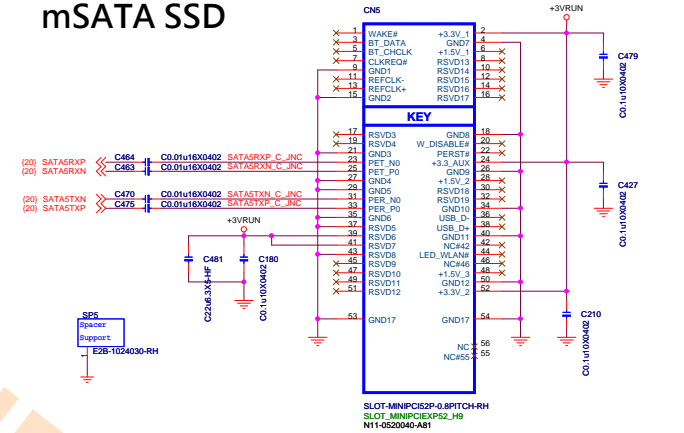
SATA HDD



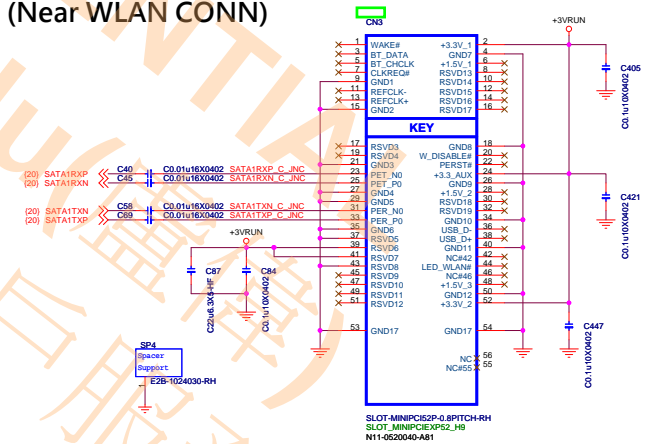
SATA ODD



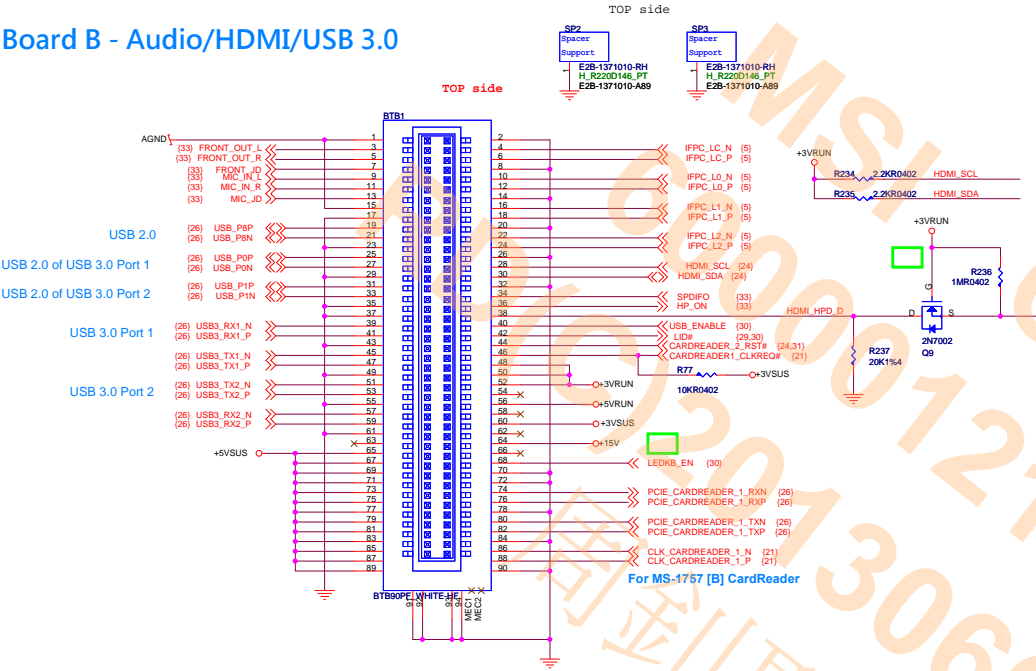
mSATA SSD



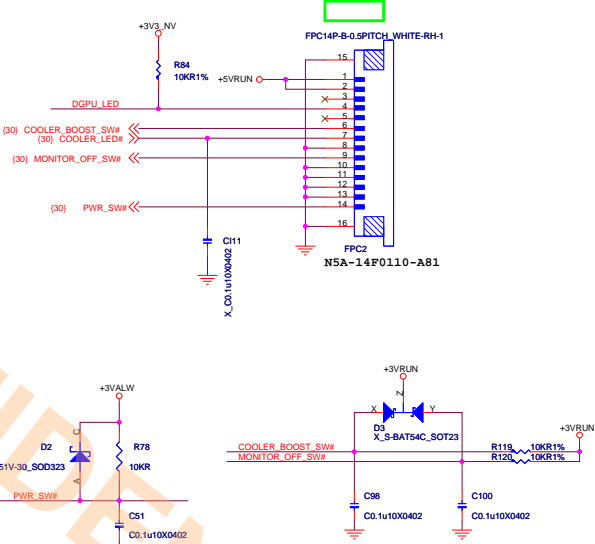
mSATA SSD
(Near WLAN CONN)



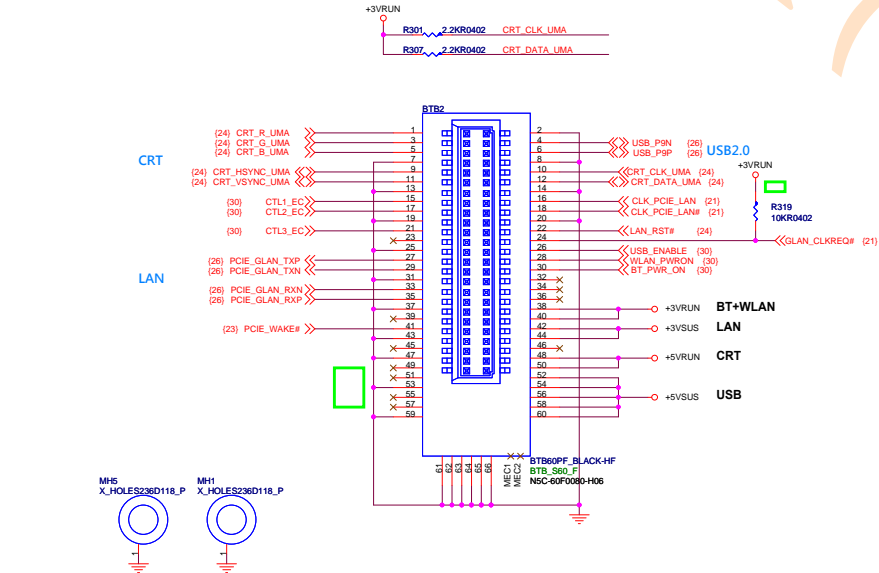
Board B - Audio/HDMI/USB 3.0



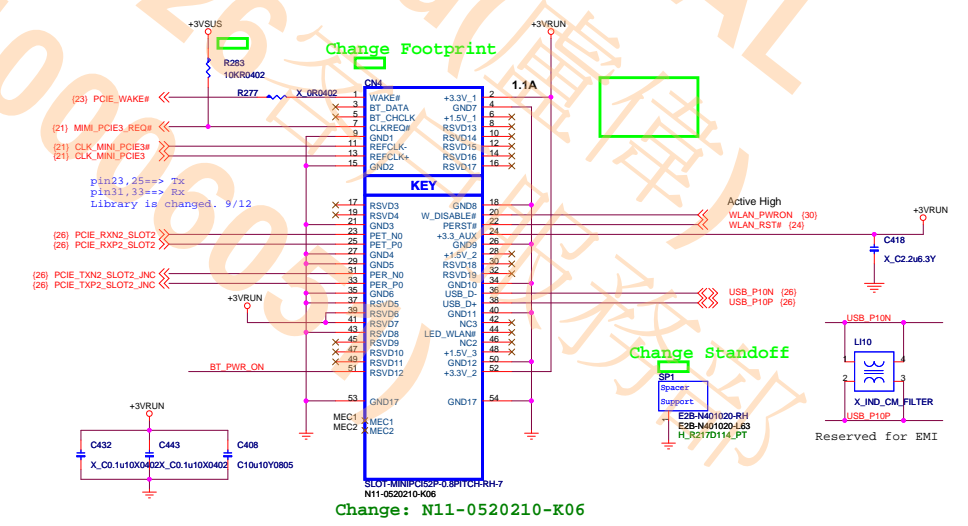
To 16GCC(Power Key Board) / FPCC1



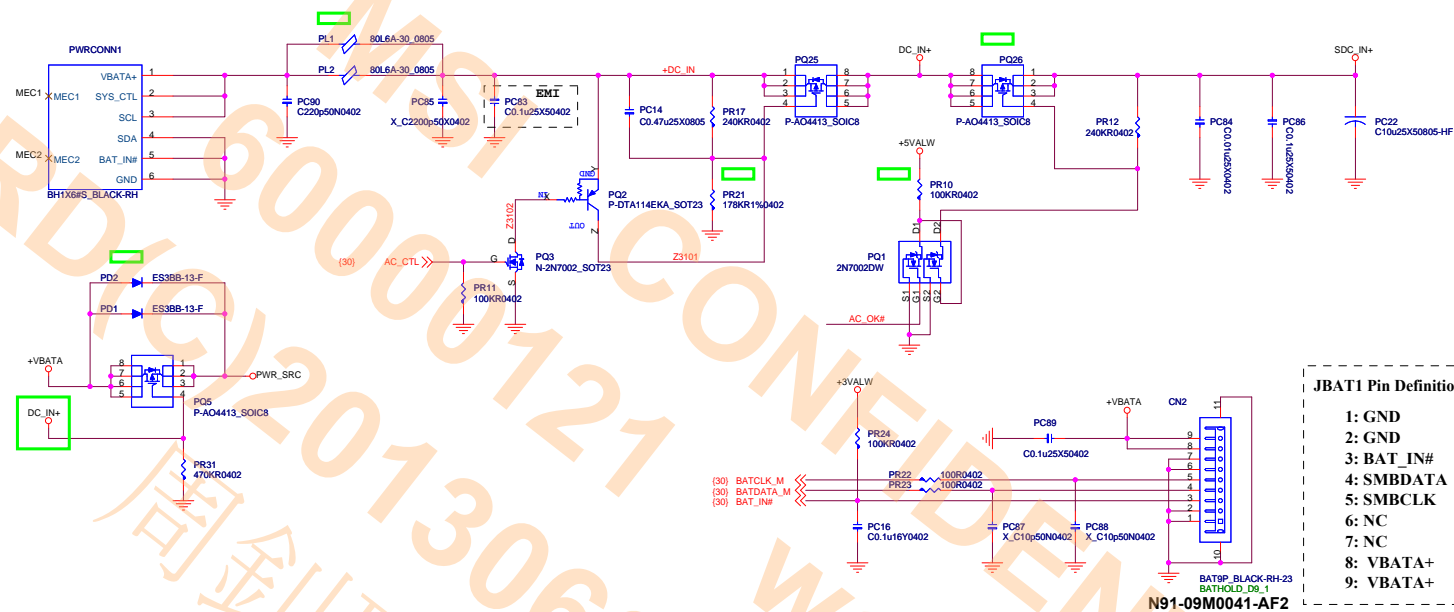
Board A - CRT/USB/WLAN/BT/LAN



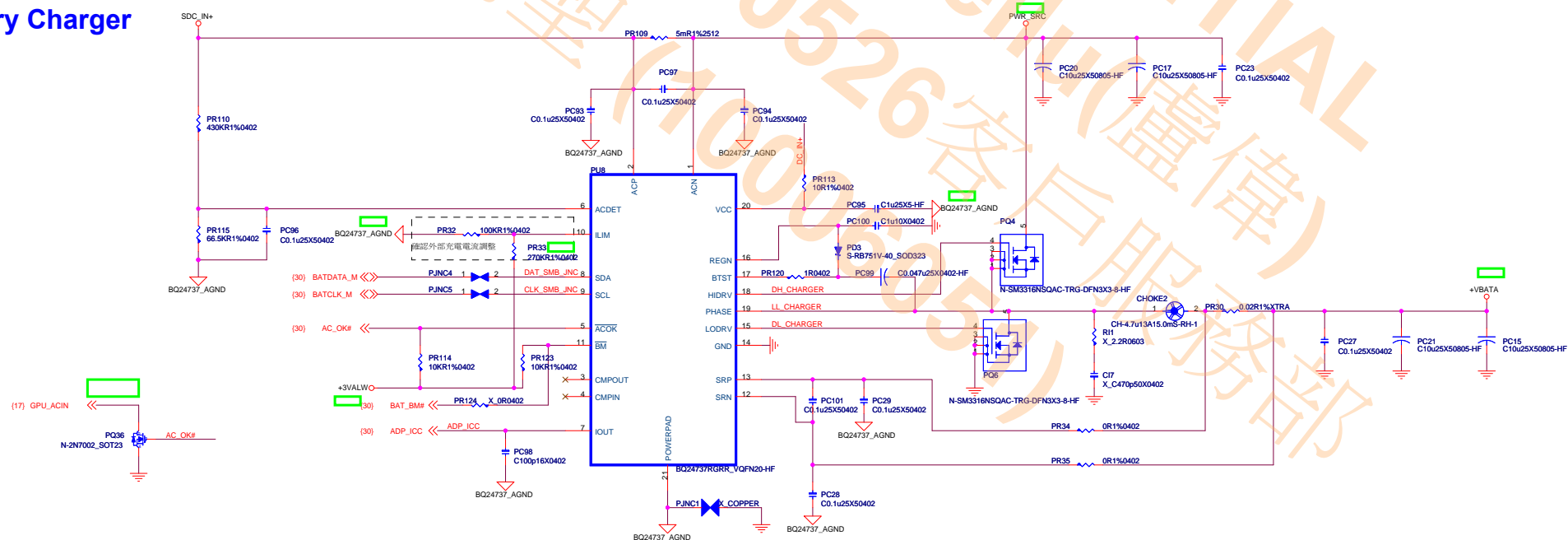
WLAN CARD



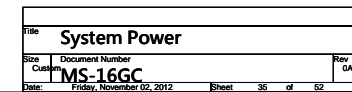
Battery Select



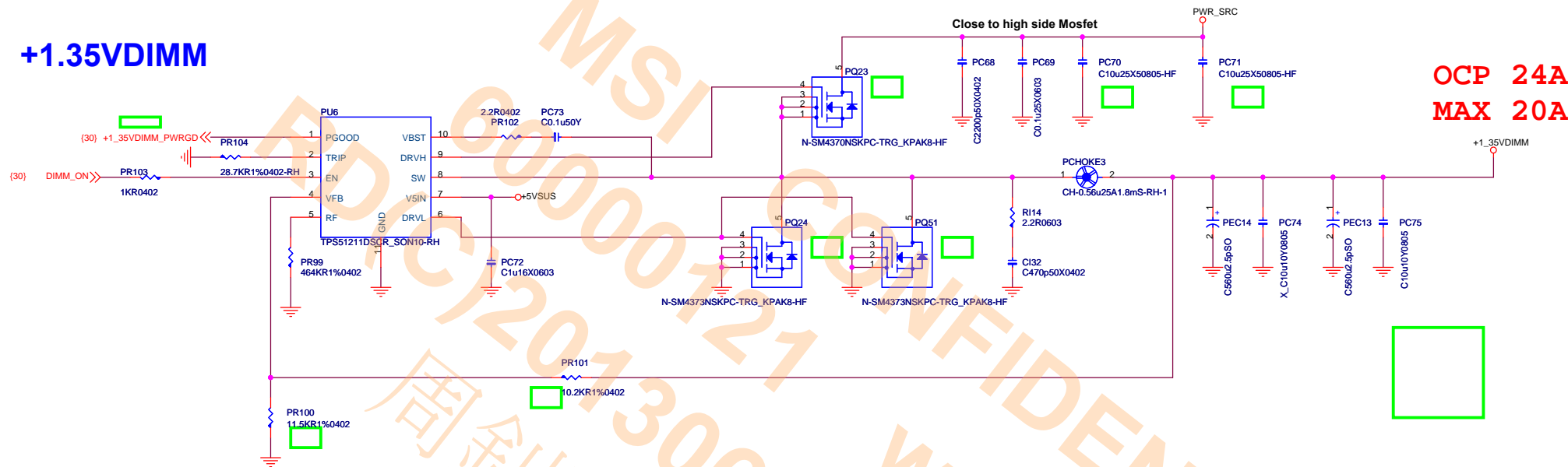
Battery Charger



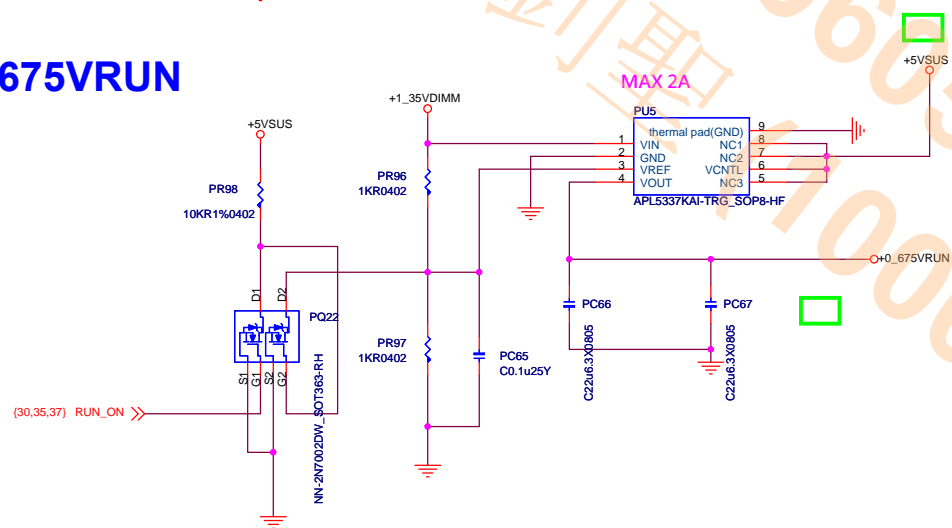
OCP 8A
MAX 6A
+3VSUS



+1.35VDIMM

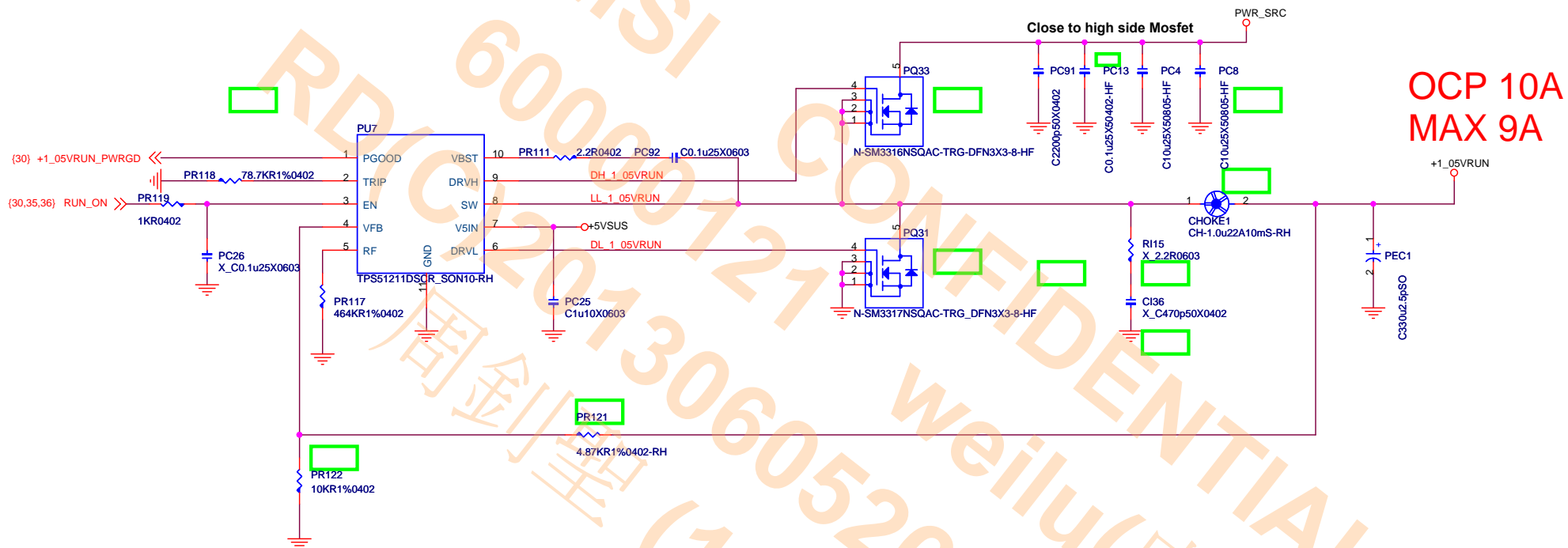


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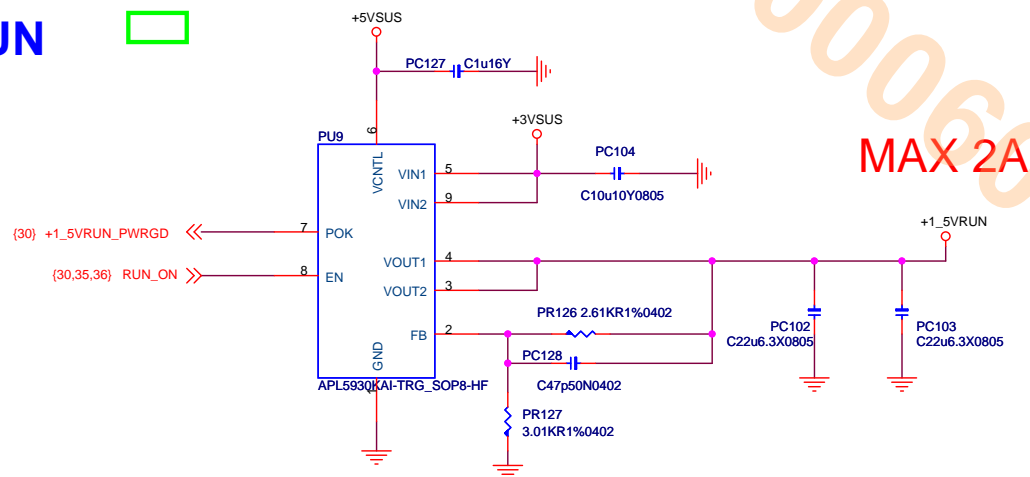


Title		+1.35VDIMM/+0.675VRUN	
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+1.05VRUN

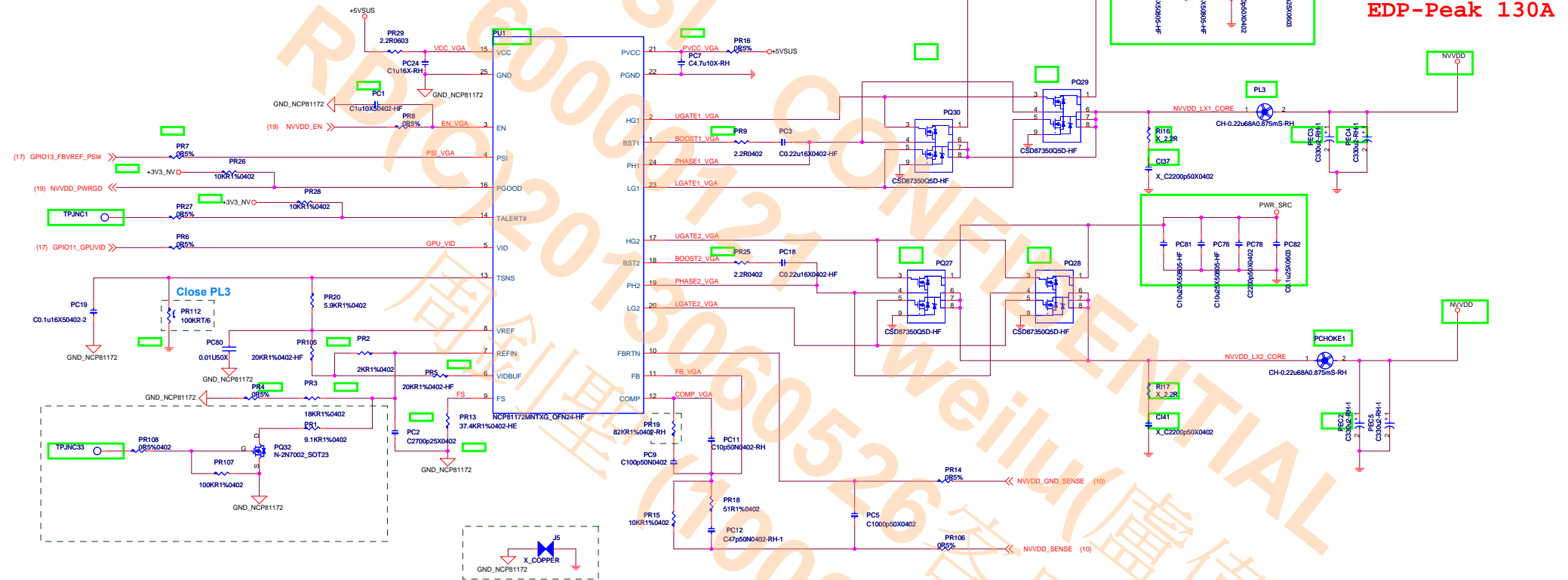


+1.5VRUN



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+1.05VRUN / +1.5VRUN		
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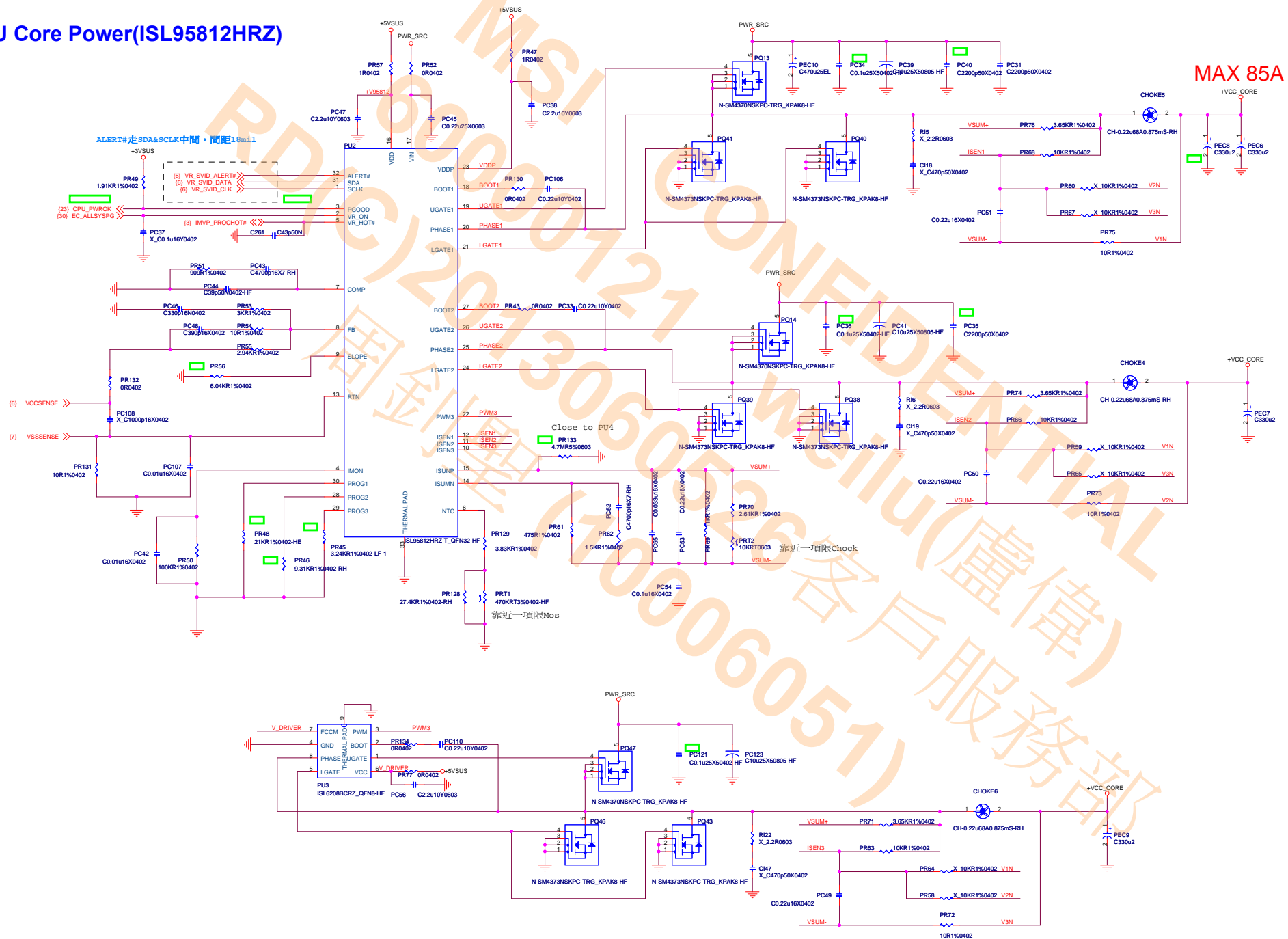
DGPU POWER / NCP81172

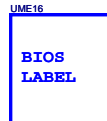
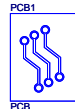
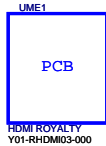
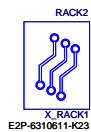
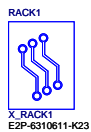
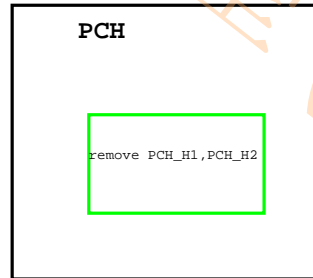
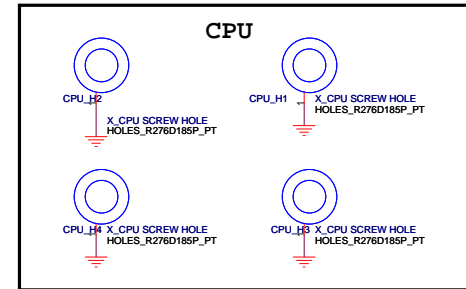
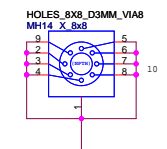
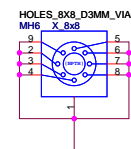
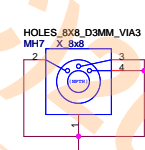
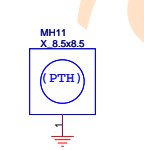
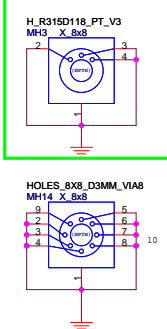
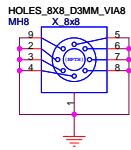
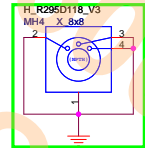
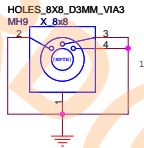
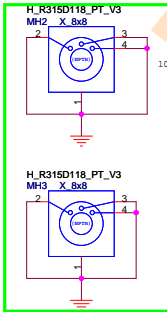
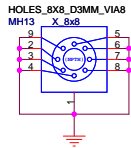


CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V
MAX 73A
EDP-Peak 130A

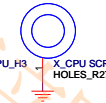
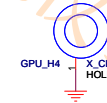
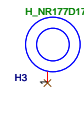
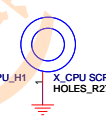
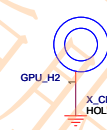
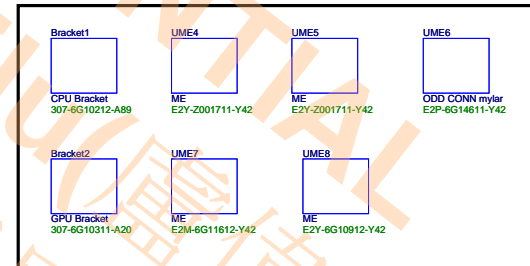
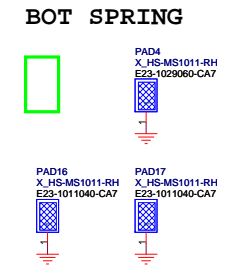
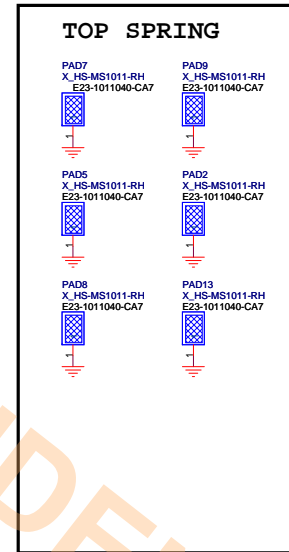
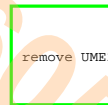
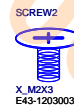
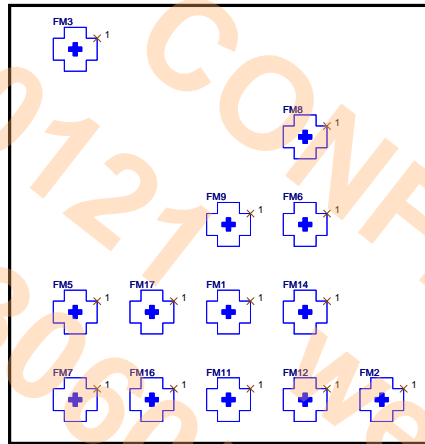
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DGPU Power			
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CPU Core Power(ISL95812HRZ)





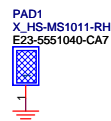
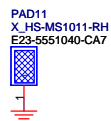
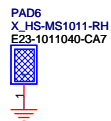
For MP: BIOS Label



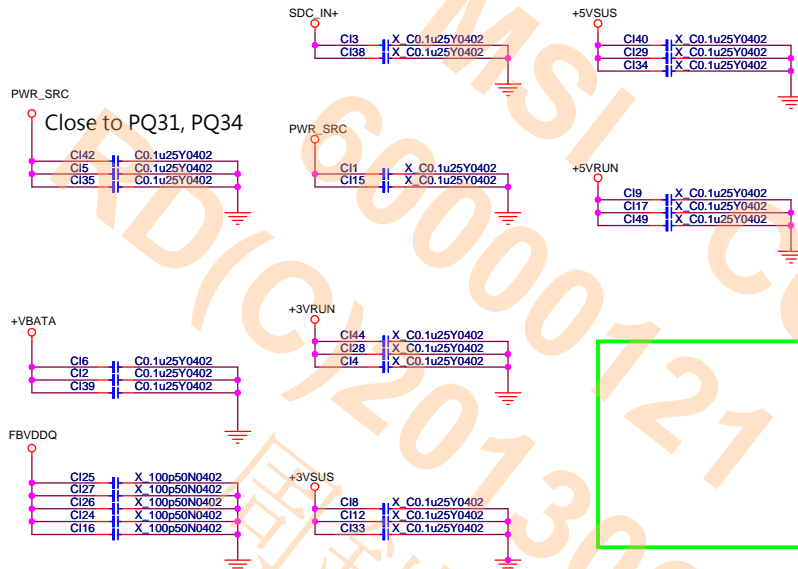
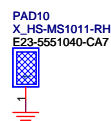
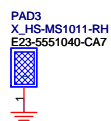
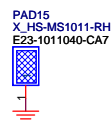
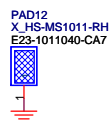
remove H8

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Screw/ME			
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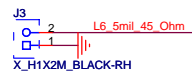
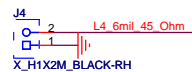
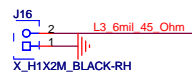
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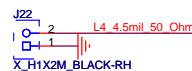
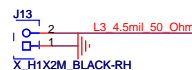
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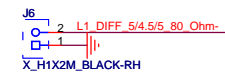
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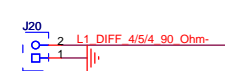
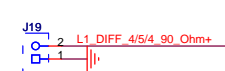
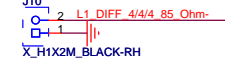
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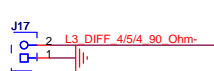
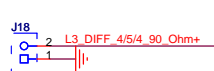
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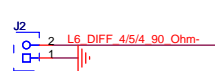
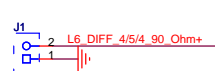
85 OHM



90 OHM

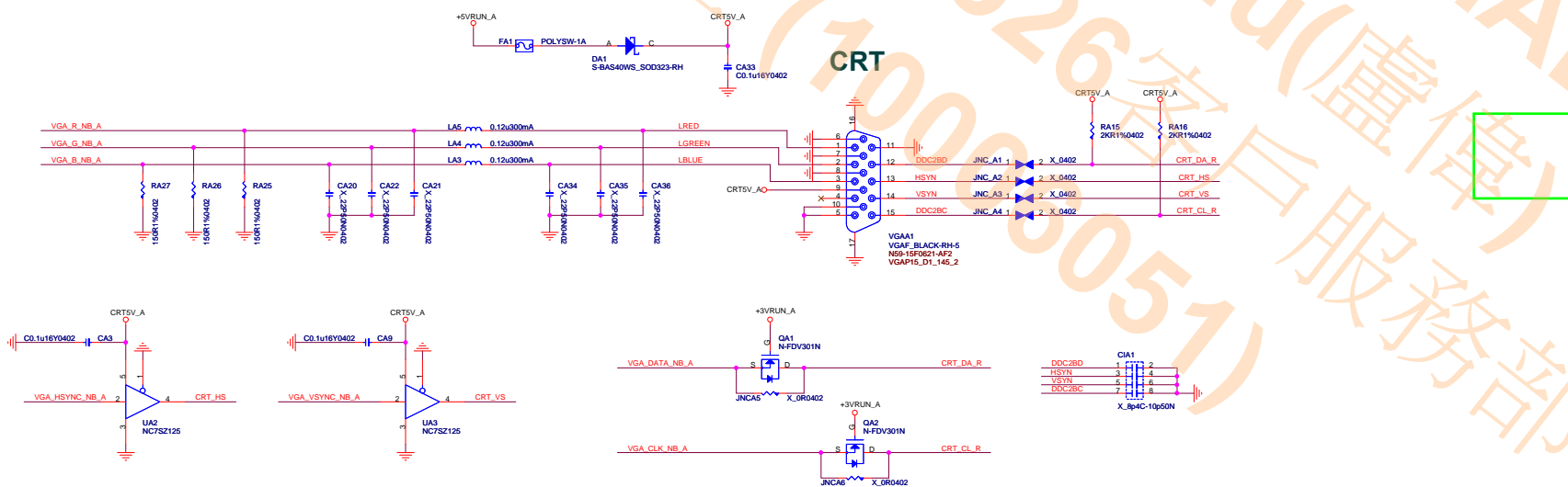
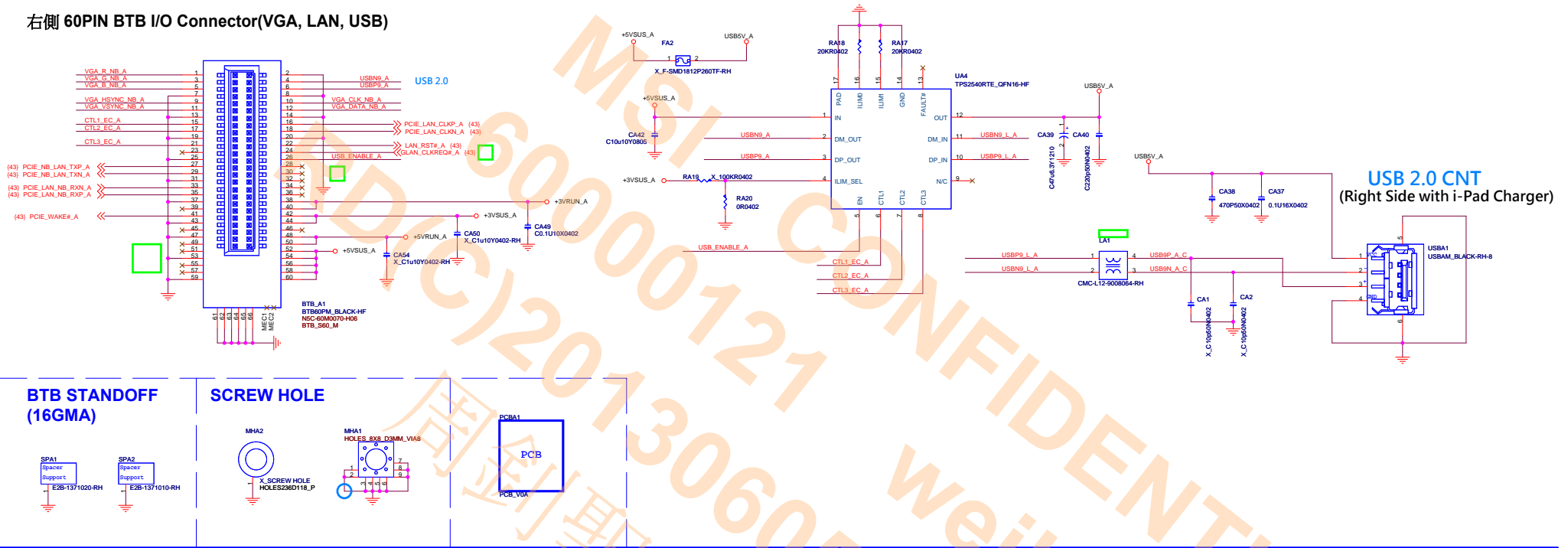


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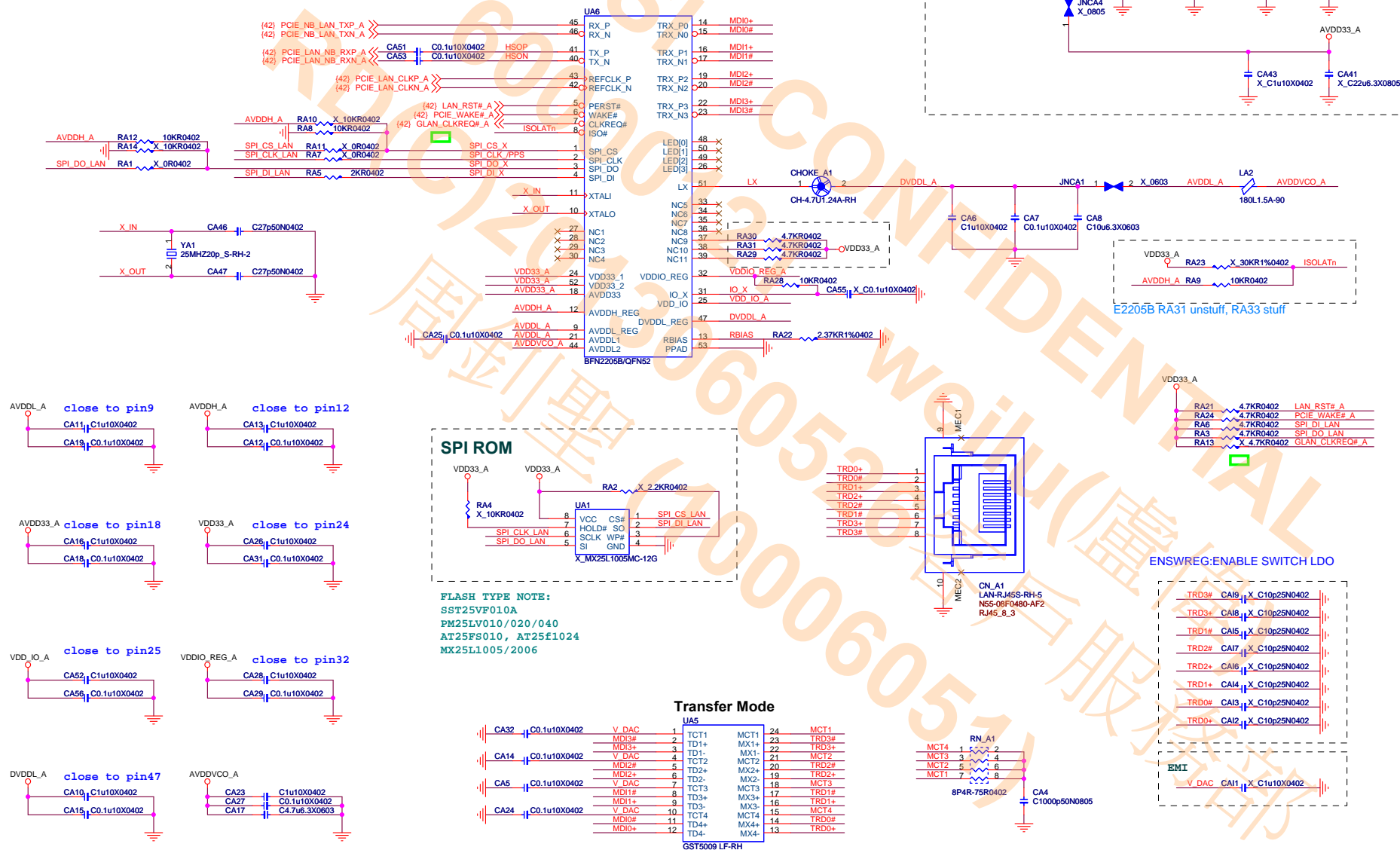
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右側 60PIN BTB I/O Connector(VGA, LAN, USB)

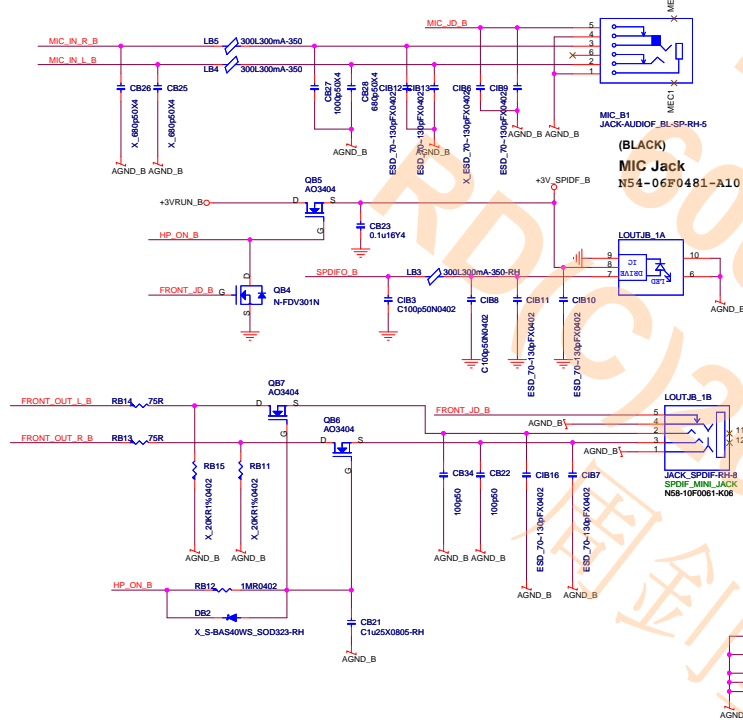


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GIGA LAN(BFN2200A)

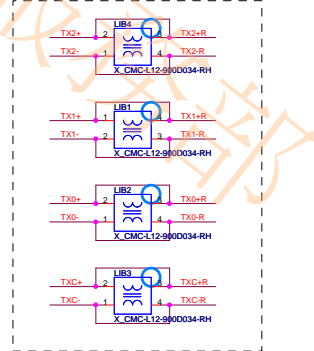
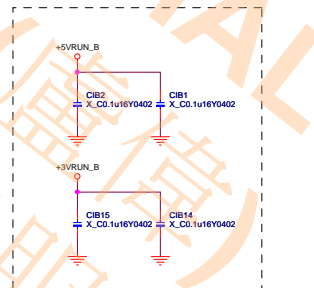
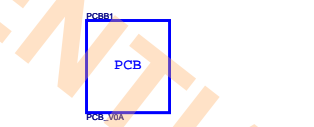
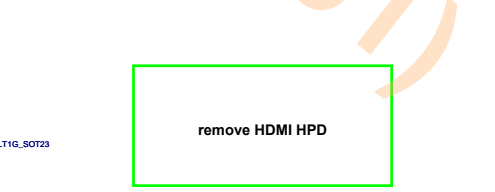
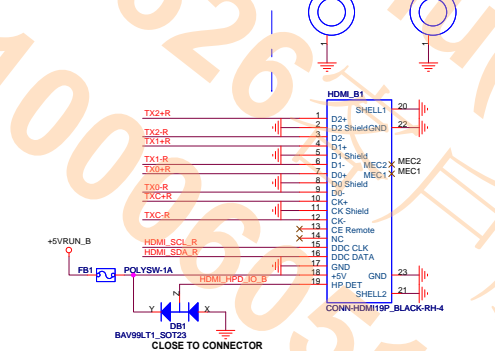
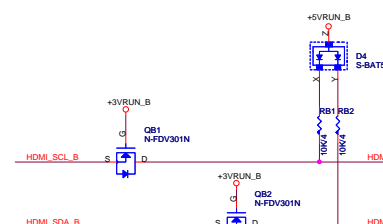
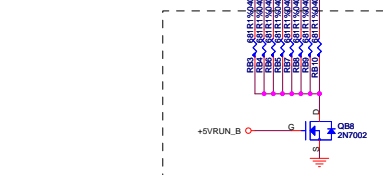
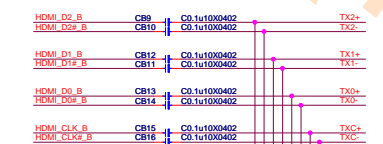
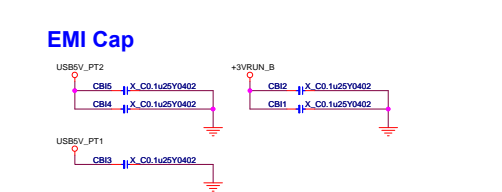
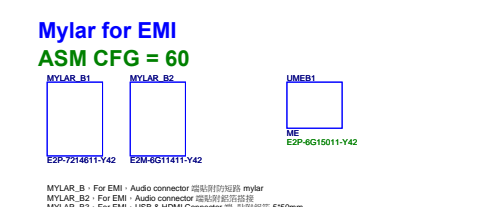
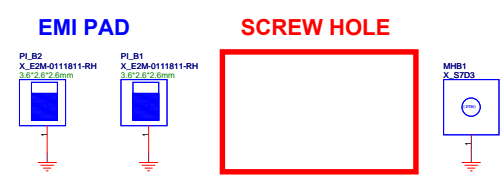
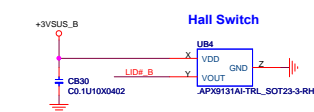
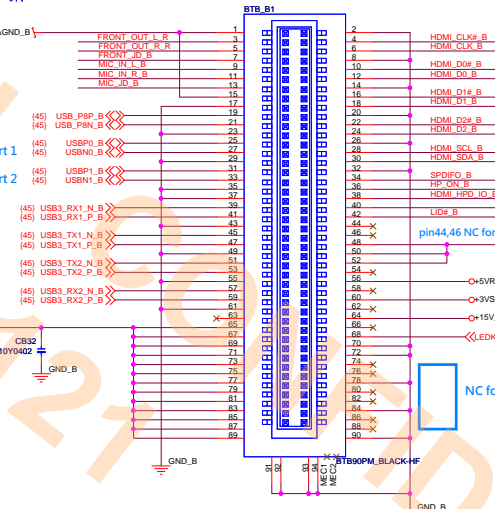


16GCB board to board CONN1: HDMI,Audio, LED,LID



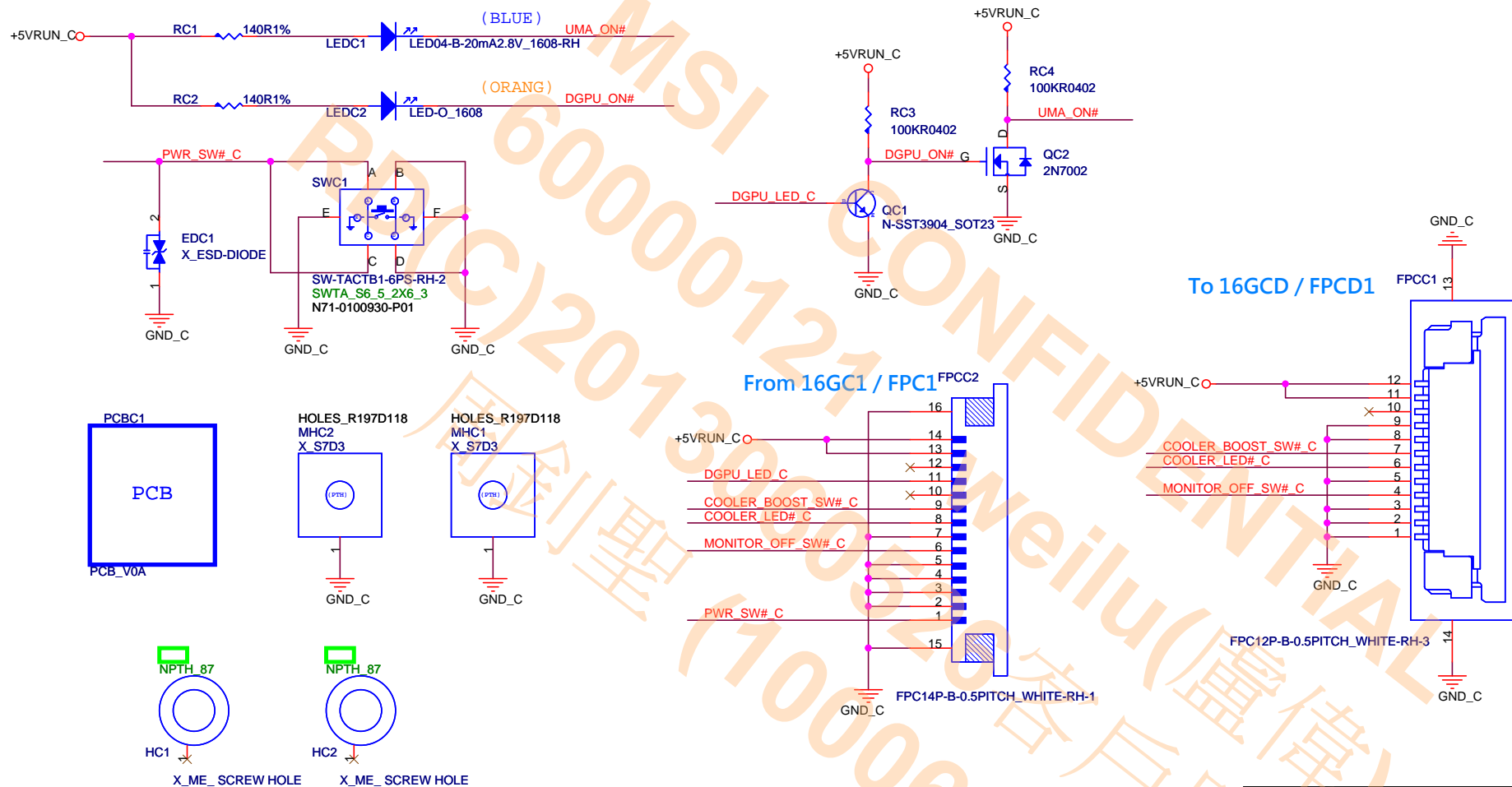
FRONT_OUT_L_B CB1 1-2 C100u6.3S50 FRONT_OUT_L_B
FRONT_OUT_R_B CB2 1-2 C100u6.3S50 FRONT_OUT_R_B

USB 2.0
USB 2.0 of USB 3.0 Port 1
USB 2.0 of USB 3.0 Port 2

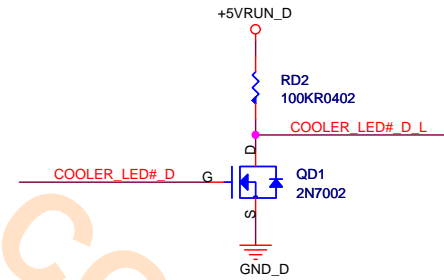
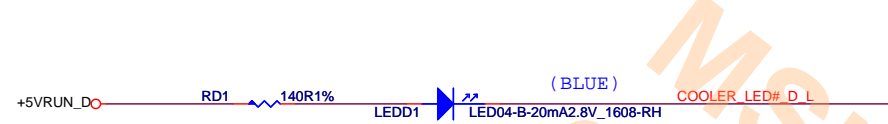




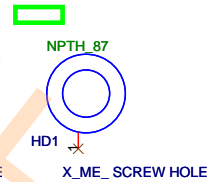
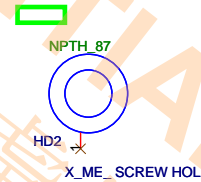
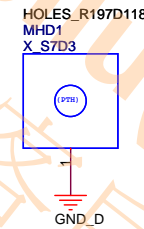
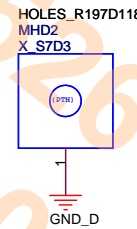
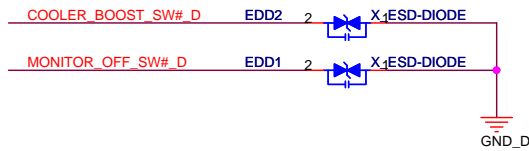
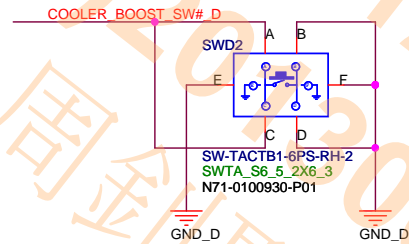
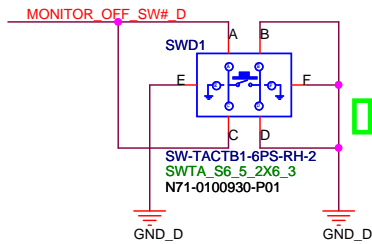
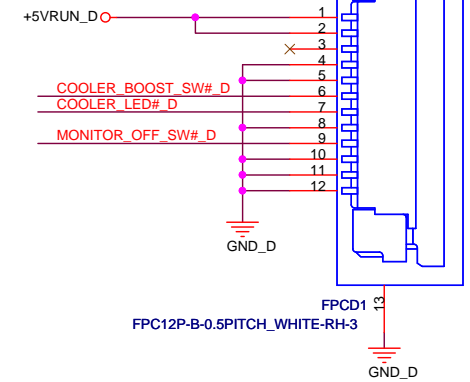
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Title			[C] Power SW Board		
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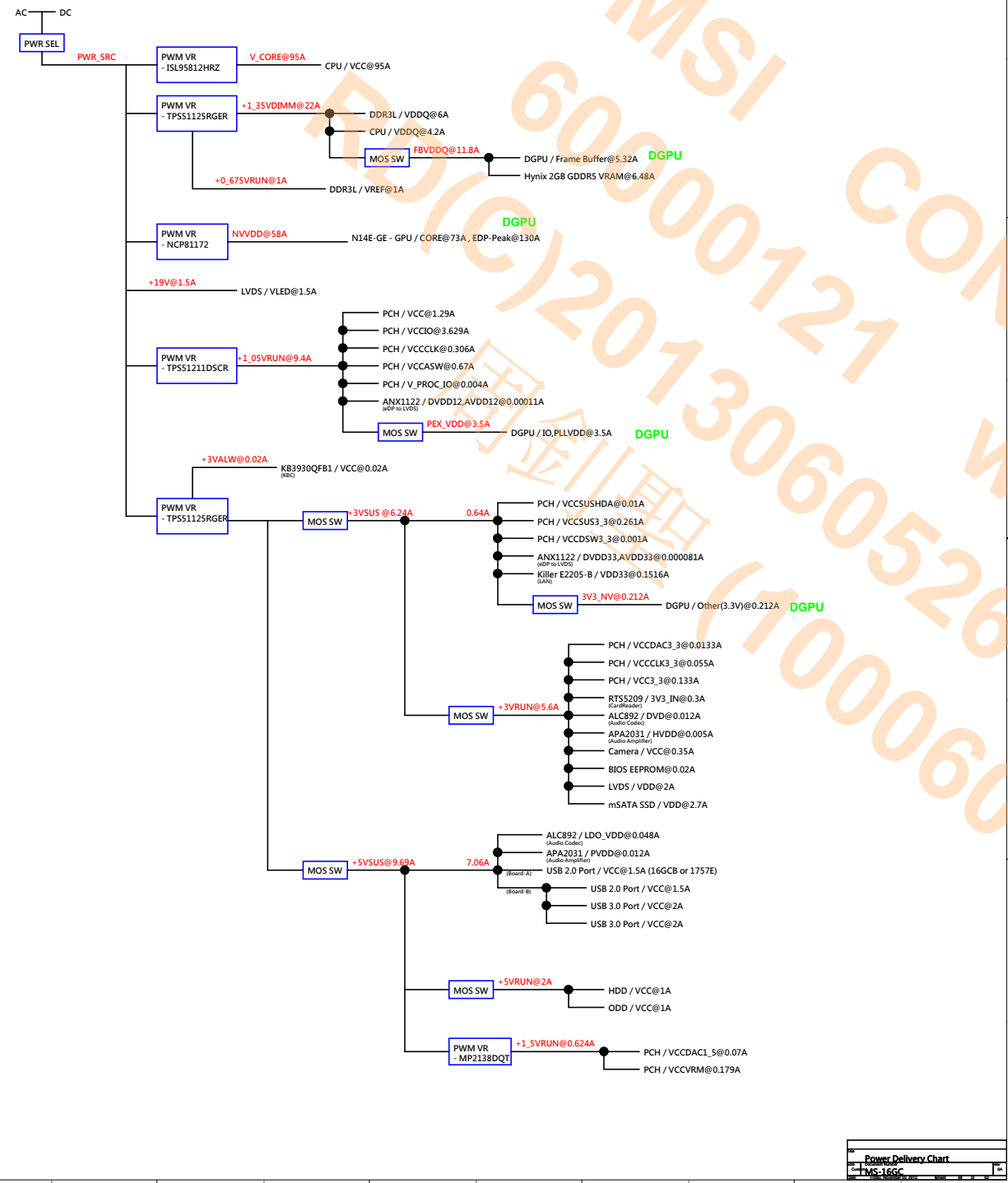


From 16GCC / FPCC1

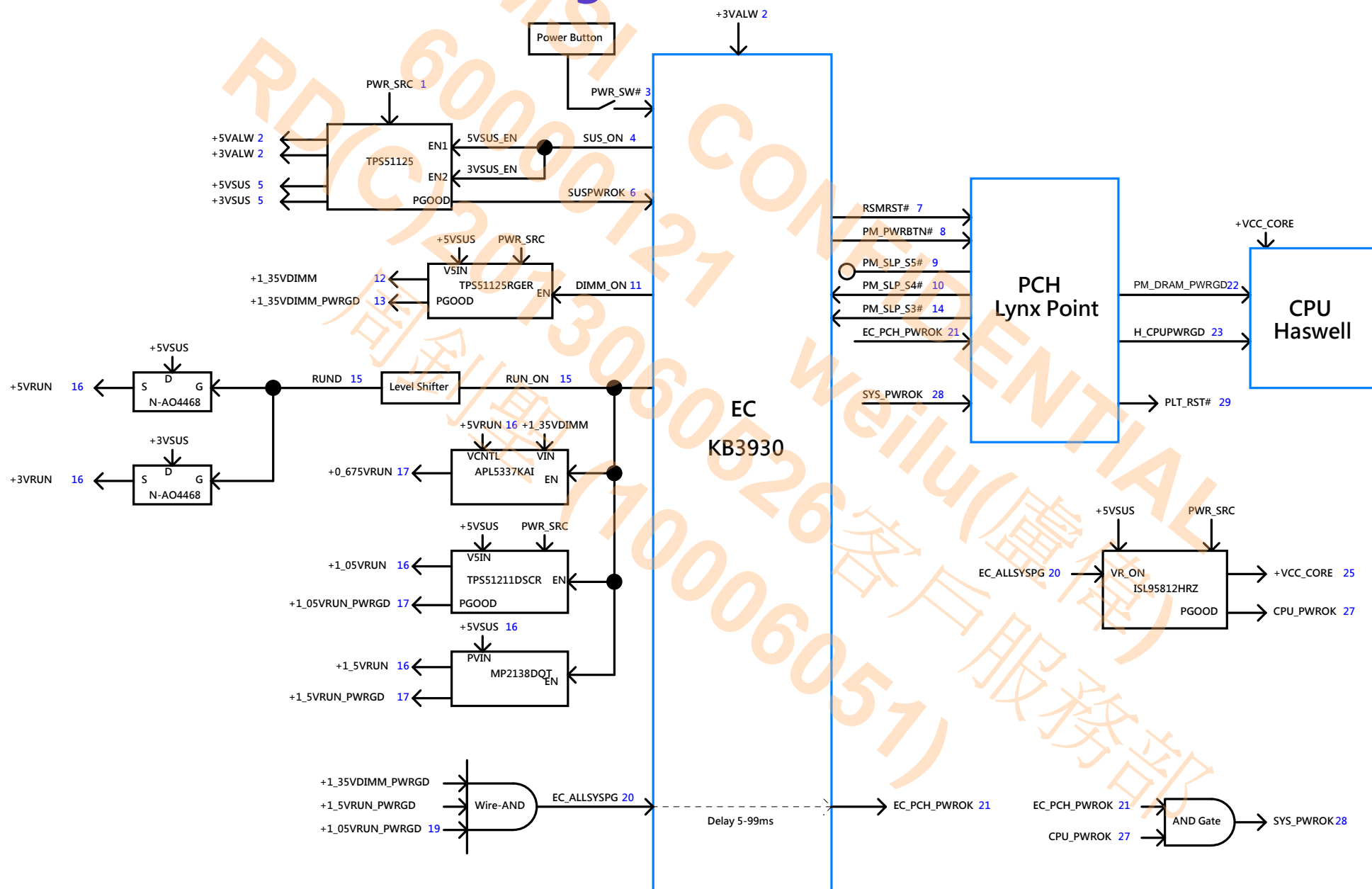


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Size			Document Number		
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16GC Power Delivery Chart

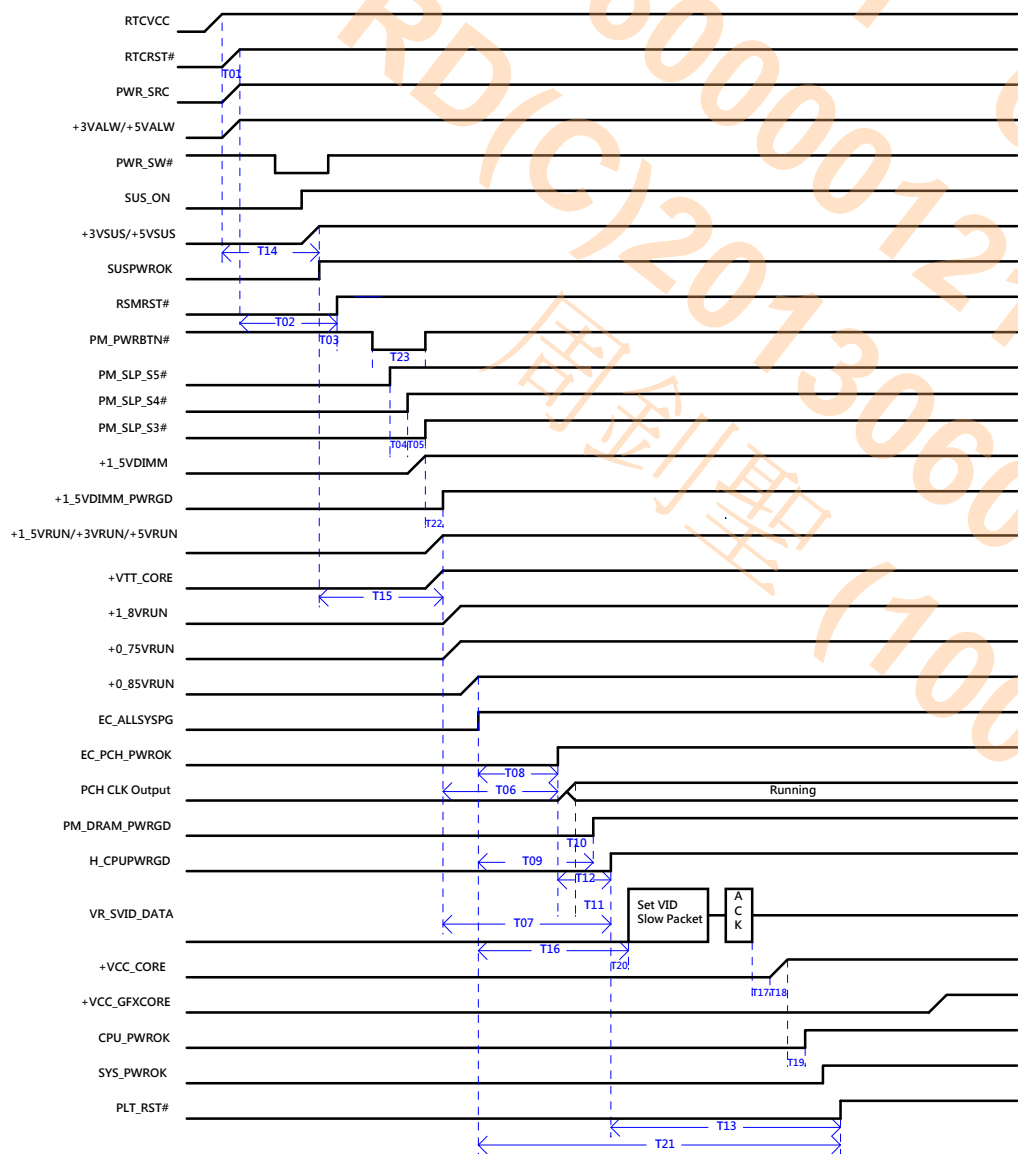


16GC Power on Block Diagram



Power on Sequence

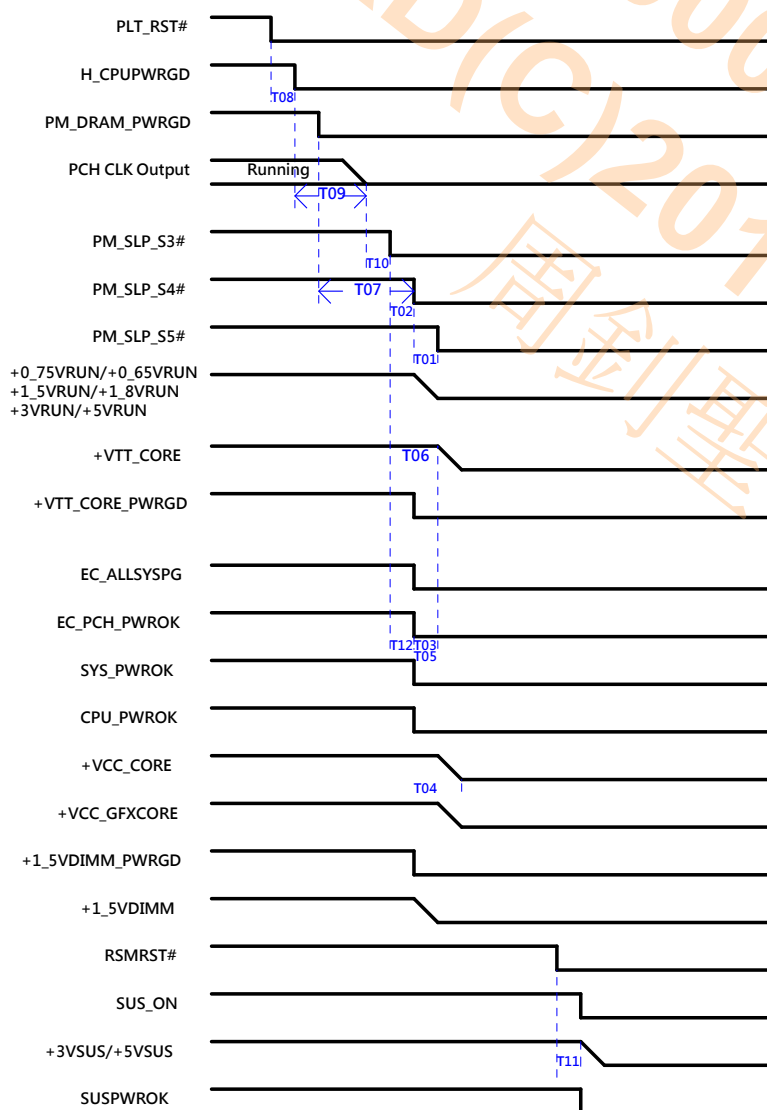
G3 -> S0



	MIN	MAX	Units	Description
T01	9		ms	RTCVCC Stable to RTCRST# de-assertion
T02	0		ms	RTCRST# de-assertion to RSMRST# de-assertion
T03	10		ms	+3VSUS/+5VSUS stable to RSMRST# de-assertion
T04	30		us	SLP_S5# de-assertion to SLP_S4# de-assertion
T05	30		us	SLP_S4# de-assertion to SLP_S3# de-assertion
T06	1		ms	+VTT_CORE stable to EC_PCH_PWROK assertion
T07	5	650	ms	+1_8VRUN stable to H_CPUPWRGD assertion
T08	99		ms	EC_ALLSYSPG assertion to EC_PCH_PWROK
T09	2	650	ms	Last CPU uncore power stable to PM_DRAM_PWRGD assertion
T10	0		us	EC_PCH_PWROK assertion to PM_DRAM_PWRGD assertion
T11	1		ms	PCH CLK output stable to H_CPUPWRGD assertion
T12	2		ms	EC_PCH_PWROK assertion to H_CPUPWRGD assertion
T13	1	100	ms	H_CPUPWRGD assertion to PLT_RST# de-assertion
T14	0		ms	RTCVCC Stable to +3VSUS/+5VSUS Stable
T15	0		ms	+3VSUS/+5VSUS Stable to +VTT_CORE Stable
T16		5	ms	EC_ALLSYSPG to CPU Core Power VR is ready to accept SVID command
T17	0	50	us	ACK of VR_SVID_DATA to +VCC_CORE starts to ramp
T18	50	2000	us	+VCC_CORE ramp time
T19		5	ms	+VCC_CORE stable to CPU_PWROK assertion
T20		500	us	H_CPUPWRGD assertion to first SVID transaction
T21	100		ms	EC_PCH_PWROK assertion to PLT_RST# de-assertion
T22	100		ns	80 % +1_5VDIMM to +1_5VDIMM_PWRGD assertion

Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	40		ns	EC_PCH_PWROK de-assertion to +VTT_CORE falling
T04		500	ms	SLP_S3# de-assertion to +VCC_CORE/+VCC_GFXCORE off
T05	40		ns	EC_PCH_PWROK de-assertion to +VTT_CORE falling
T06	5		us	SLP_S3# de-assertion to +VTT_CORE falling
T07	100		ns	PM_DRAM_PWRGD de-assertion to SLP_S4# assertion
T08	30		us	PLT_RST# assertion to H_CPUPWRGD de-assertion
T09	10		us	H_CPUPWRGD de-assertion to PCH CLK output off
T10	0		us	PCH CLK Output off to SLP_S3# assertion
T11	40		ns	RSMRST# assertion to +3VSUS/+5VSUS falling
T12	0		ms	SLP_S3# assertion to EC_PCH_PWROK de-assertion

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